



BSI Standards Publication

Semiconductor devices - Mechanical and climatic test methods

Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM)(IEC 60749-26:2018)

National foreword

This British Standard is the UK implementation of EN IEC 60749-26:2018. It is identical to IEC 60749-26:2018. It supersedes BS EN 60749-26:2014, which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

A list of organizations represented on this committee can be obtained on request to its secretary.

This publication does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

© The British Standards Institution 2018
Published by BSI Standards Limited 2018

ISBN 978 0 580 97604 9

ICS 31.080.01

Compliance with a British Standard cannot confer immunity from legal obligations.

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 30 April 2018.

Amendments/corrigenda issued since publication

Date	Text affected
------	---------------

EUROPEAN STANDARD

EN IEC 60749-26

NORME EUROPÉENNE

EUROPÄISCHE NORM

March 2018

ICS 31.080.01

Supersedes EN 60749-26:2014

English Version

**Semiconductor devices - Mechanical and climatic test methods -
Part 26: Electrostatic discharge (ESD) sensitivity testing -
Human body model (HBM)
(IEC 60749-26:2018)**

Dispositifs à semiconducteurs - Méthodes d'essais
mécaniques et climatiques - Partie 26: Essai de sensibilité
aux décharges électrostatiques (DES) - Modèle du corps
humain (HBM)
(IEC 60749-26:2018)

Halbleiterbauelemente - Mechanische und klimatische
Prüfverfahren - Teil 26: Prüfung der Empfindlichkeit gegen
elektrostatische Entladungen (ESD) - Human Body Model
(HBM)
(IEC 60749-26:2018)

This European Standard was approved by CENELEC on 2018-02-19. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Serbia, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.



European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Rue de la Science 23, B-1040 Brussels

European foreword

The text of document 47/2438/FDIS, future edition 4 of IEC 60749-26, prepared by IEC/TC 47 "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 60749-26:2018.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2018-11-19
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2021-02-19

This document supersedes EN 60749-26:2014.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 60749-26:2018 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60749 (series)	NOTE	Harmonized as EN 60749 (series).
IEC 60749-27	NOTE	Harmonized as EN 60749-27.

CONTENTS

FOREWORD.....	5
1 Scope.....	7
2 Normative references	7
3 Terms and definitions	7
4 Apparatus and required equipment.....	10
4.1 Waveform verification equipment	10
4.2 Oscilloscope	11
4.3 Additional requirements for digital oscilloscopes	11
4.4 Current transducer (inductive current probe).....	11
4.5 Evaluation loads	11
4.6 Human body model simulator	12
4.7 HBM test equipment parasitic properties	12
5 Stress test equipment qualification and routine verification	12
5.1 Overview of required HBM tester evaluations	12
5.2 Measurement procedures.....	13
5.2.1 Reference pin pair determination	13
5.2.2 Waveform capture with current probe	13
5.2.3 Determination of waveform parameters.....	14
5.2.4 High voltage discharge path test.....	17
5.3 HBM tester qualification	17
5.3.1 HBM ESD tester qualification requirements	17
5.3.2 HBM tester qualification procedure	17
5.4 Test fixture board qualification for socketed testers	18
5.5 Routine waveform check requirements.....	19
5.5.1 Standard routine waveform check description	19
5.5.2 Waveform check frequency.....	19
5.5.3 Alternate routine waveform capture procedure	20
5.6 High voltage discharge path check.....	20
5.6.1 Relay testers	20
5.6.2 Non-relay testers	20
5.7 Tester waveform records.....	20
5.7.1 Tester and test fixture board qualification records.....	20
5.7.2 Periodic waveform check records	20
5.8 Safety	21
5.8.1 Initial set-up.....	21
5.8.2 Training	21
5.8.3 Personnel safety.....	21
6 Classification procedure	21
6.1 Devices for classification	21
6.2 Parametric and functional testing	21
6.3 Device stressing	21
6.4 Pin categorization	22
6.4.1 General	22
6.4.2 No connect pins.....	22
6.4.3 Supply pins.....	23
6.4.4 Non-supply pins.....	23

6.5	Pin groupings.....	24
6.5.1	Supply pin groups.....	24
6.5.2	Shorted non-supply pin groups.....	24
6.6	Pin stress combinations.....	24
6.6.1	Pin stress combination categorization.....	24
6.6.2	Non-supply and supply to supply combinations (1, 2, ... N).....	26
6.6.3	Non-supply to non-supply combinations.....	27
6.7	HBM stressing with a low-parasitic simulator.....	28
6.7.1	Low-parasitic HBM simulator.....	28
6.7.2	Requirements for low parasitics.....	28
6.8	Testing after stressing.....	28
7	Failure criteria.....	28
8	Component classification.....	28
Annex A (informative) HBM test method flow chart.....		30
Annex B (informative) HBM test equipment parasitic properties.....		33
B.1	Optional trailing pulse detection equipment / apparatus.....	33
B.2	Optional pre-pulse voltage rise test equipment.....	34
B.3	Open-relay tester capacitance parasitics.....	36
B.4	Test to determine if an HBM simulator is a low-parasitic simulator.....	36
Annex C (informative) Example of testing a product using Table 2, Table 3, or Table 2 with a two-pin HBM tester.....		38
C.1	General.....	38
C.2	Procedure A (following Table 2):.....	39
C.3	Alternative procedure B (following Table 3):.....	40
C.4	Alternative procedure C (following Table 2):.....	41
Annex D (informative) Examples of coupled non-supply pin pairs.....		43
Annex E (normative) Cloned non-supply (I/O) pin sampling test method.....		44
E.1	Purpose and overview.....	44
E.2	Pin sampling overview and statistical details.....	44
E.3	IC product selections.....	45
E.4	Randomly selecting and testing cloned I/O pins.....	46
E.5	Determining if sampling can be used with the supplied Excel spreadsheet.....	46
E.5.1	Using the supplied Excel spreadsheet.....	46
E.5.2	Without using the Excel spreadsheet.....	46
E.6	HBM testing with a sample of cloned I/O pins.....	46
E.7	Examples of testing with sampled cloned I/Os.....	47
Bibliography.....		50
Figure 1 – Simplified HBM simulator circuit with loads.....		12
Figure 2 – Current waveform through shorting wires.....		15
Figure 3 – Current waveform through a 500 Ω resistor.....		16
Figure 4 – Peak current short circuit ringing waveform.....		17
Figure A.1 – HBM test method flow chart (1 of 3).....		30
Figure B.1 – Diagram of trailing pulse measurement setup.....		33
Figure B.2 – Positive stress at 4 000 V.....		34
Figure B.3 – Negative stress at 4 000 V.....		34

Figure B.4 – Illustration of measuring voltage before HBM pulse with a Zener diode or a device	35
Figure B.5 – Example of voltage rise before the HBM current pulse across a 9,4 V Zener diode	35
Figure B.6 – Diagram of a 10-pin shorting test device showing current probe.....	37
Figure C.1 – Example to demonstrate the idea of the partitioned test.....	38
Figure E.1 – SPL, V1, VM, and z with the Bell shape distribution pin failure curve	45
Figure E.2 – I/O sampling test method flow chart	49
Table 1 – Waveform specification	19
Table 2 – Preferred pin combinations sets	25
Table 3 – Alternative pin combinations sets	26
Table 4 – HBM ESD component classification levels.....	29
Table C.1 – Product testing in accordance with Table 2	40
Table C.2 – Product testing in accordance with Table 3	41
Table C.3 – Alternative product testing in accordance with Table 2.....	42

INTERNATIONAL ELECTROTECHNICAL COMMISSION

**SEMICONDUCTOR DEVICES –
MECHANICAL AND CLIMATIC TEST METHODS –****Part 26: Electrostatic discharge (ESD) sensitivity testing –
Human body model (HBM)**

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60749-26 has been prepared by IEC technical committee 47: Semiconductor devices in collaboration with technical committee 101: Electrostatics.

This fourth edition cancels and replaces the third edition published in 2013. This edition constitutes a technical revision. This standard is based upon ANSI/ESDA/JEDEC JS-001-2014. It is used with permission of the copyright holders, ESD Association and JEDEC Solid state Technology Association.

This edition includes the following significant technical changes with respect to the previous edition:

- a) a new subclause relating to HBM stressing with a low parasitic simulator is added, together with a test to determine if an HBM simulator is a low parasitic simulator;

- b) a new subclause is added for cloned non-supply pins and a new annex is added for testing cloned non-supply pins.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/2438/FDIS	47/2454/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)

1 Scope

This part of IEC 60749 establishes the procedure for testing, evaluating, and classifying components and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD).

The purpose of this document is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of component type. Repeatable data will allow accurate classifications and comparisons of HBM ESD sensitivity levels.

ESD testing of semiconductor devices is selected from this test method, the machine model (MM) test method (see IEC 60749-27) or other ESD test methods in the IEC 60749 series. Unless otherwise specified, this test method is the one selected.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1

associated non-supply pin

non-supply pin (typically an I/O pin) associated with a supply pin group

Note 1 to entry A non-supply pin is considered to be associated with a supply pin group if either:

- a) the current from the supply pin group (i.e., VDDIO) is required for the function of the electrical circuit(s) (I/O driver) that connect(s) (high/low impedance) to that non-supply pin;
- b) a parasitic path exists between non-supply and supply pin group (e.g., open-drain type non-supply pin to a VCC supply pin group that connects to a nearby N-well guard ring).