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TECHNICAL REPORT

colour inside

Process management for avionics – Electronic components capability in operation –
Part 2: Semiconductor microcircuit lifetime

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CONTENTS

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PROCESS MANAGEMENT FOR AVIONICS – ELECTRONIC COMPONENTS CAPABILITY IN OPERATION –

Part 2: Semiconductor microcircuit lifetime

FOREWORD

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IEC TR 62240-2, which is a Technical Report, has been prepared by IEC technical committee 107: Process management for avionics.

IEC TR 62240-2 adapts and modifies the GIFAS/2015/5022 document that has served as a basis for the elaboration of this Technical Report.

The text of this Technical Report is based on the following documents:

Draft TR	Report on voting
107/325/DTR	107/332/RVDTR

Full information on the voting for the approval of this Technical Report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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INTRODUCTION

Electronic equipment for aerospace, defence and high performance (ADHP) applications integrate more and more commercial off the shelf (COTS) semiconductor microcircuits. These semiconductor microcircuits are above all designed and produced to address high volume and low cost markets such as consumer electronics, telecommunications or microcomputers, whose main requirements are basically cost, integration, performance and low consumption and for which the long term reliability in severe environments (for example vibration, thermal cycling, humidity and operating temperature) is not necessarily an imperative design criterion.

With semiconductor transistor feature size decrease, mainly from 90 nm transistor feature size, early wear-out can arise in COTS semiconductor microcircuits. For example, non-homothetic evolution of semiconductor microcircuit bias voltage and transistor feature size scaling have led to an increase of the electrical fields inside the semiconductor microcircuit and hence changes in classical failure and degradation modes or mechanisms. In addition new transistor architectures and technologies (for example fin field effect transistor (FinFET), fully depleted silicon on insulator (FD-SOI), etc.) and new materials (for example low-k dielectrics, high-k dielectrics, strain source/drain Si-Ge) have been introduced since the generation 90 nm to overcome the scaling issues, contributing potentially to the evolution of failure and degradation modes or mechanisms.

In this context, the lifetime of new generations of COTS semiconductor microcircuits may not meet the lifetime requirements of high performance, high reliability and long duration electronic applications (for example twenty years, thirty years or more). As a consequence, specific reliability assessment and maintenance plans are considered within the semiconductor microcircuit selection activities.

PROCESS MANAGEMENT FOR AVIONICS – ELECTRONIC COMPONENTS CAPABILITY IN OPERATION –

Part 2: Semiconductor microcircuit lifetime

1 Scope

This part of IEC 62240, which is a Technical Report, focuses on original equipment manufacturers (OEMs) using commercial off the shelf (COTS) semiconductor microcircuits for high performance, high reliability and long duration applications. This document supports OEMs in the preparation and maintenance of their semiconductor electronic component management plan (ECMP).

This document describes a process and a method for selecting digital semiconductor microcircuits by ensuring that their lifetime is compatible with the requirements of aerospace, defence and high performance (ADHP) applications (generally in connection with functional environments). Methods and guidelines are provided to assess the long term reliability of COTS semiconductor microcircuits in such applications; they mainly apply during the electronic design phase when selecting semiconductor microcircuits and assessing the application reliability.

Moreover, the document focuses on the intrinsic wear-out and the lifetime of COTS semiconductor microcircuits processed of less than or equal to 90 nm feature size (also called deep sub-micron (DSM) semiconductor microcircuits) and puts aside, at this time, packaging wear-out and random failure mechanisms. In this view, physics of failure (PoF) is at the heart of the approach.

NOTE 1 IEC 62239-1 can assist OEMs in the creation and maintenance of ECMPs.

NOTE 2 SAE ARP6338 can also help the OEM with regard to assessment and mitigation of early wear-out of life-limited semiconductor microcircuits.

NOTE 3 With the evolution of electronic technology and semiconductor microcircuits processed of less than or equal to 90 nm feature size, the current MIL-HDBK-217 handbook or FIDES guide become inappropriate as they are based for the time being on the assumption that the semiconductor electronic component exhibits a constant (random) failure rate and does not have life limits or exhibit wear-out.

Moreover, silicon itself has fundamentally very low failures in time (FIT) rates and the major failure modes are often in the packaging (for example housing, bond wires, etc.).

2 Normative references

There are no normative references in this document.

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
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