# IEEE Standard VHDL Language Reference Manual

## IEEE Computer Society

Sponsored by the
Design Automation Standards Committee

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(Revision of
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**Design Automation Standards Committee**
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**IEEE Computer Society**

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**Abstract**: VHSIC Hardware Description Language (VHDL) is defined. VHDL is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine readable and human readable, it supports the development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware. Its primary audiences are the implementors of tools supporting the language and the advanced users of the language.

**Keywords:** computer languages, electronic systems, hardware, hardware design, VHDL

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# Introduction

This introduction is not part of IEEE Std 1076-2008, IEEE Standard VHDL Language Reference Manual.

The VHSIC Hardware Description Language (VHDL) is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine readable and human readable, it supports the development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware.

This document, IEEE Std 1076-2008, is a revision of IEEE Std 1076-2002 as amended by IEEE Std 1076c™-2007. Initial work on gathering requirements and developing language extensions was undertaken by the IEEE VHDL Analysis and Standardization Group (VASG), otherwise known as the 1076 Working Group. Subsequently, Accellera[a] sponsored an effort to complete that work and draft a revised Language Reference Manual. That draft was returned to IEEE for final revision and approval, resulting in this document and the associated machine-readable files. This revision incorporates numerous enhancements, both major and minor, to previously existing language feaures and several new language features. The changes are summarized in Annex E. In addition, several VHDL library packages that were previously defined in separate standards are now defined in this standard, ensuring that they are treated as integral parts of the language. Finally, this revision incorporates the IEEE Property Specification Language (PSL) as part of VHDL. The combination of these changes significantly improves VHDL as a language for specification, design, and verification of complex electronic systems.

The maintenance of the VHDL language standard is an ongoing process. The chair of the VHDL Analysis and Standardization Group extends his gratitude to all who have participated in this revision, both in the IEEE committees and the Accellera effort, and encourages the participation of all interested parties in future language revisions.[b]

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# IEEE Standard VHDL Language Reference Manual



## 1. Overview

### 1.1 Scope

This standard revises and enhances the VHDL language reference manual (LRM) by including a standard C language interface specification; specifications from previously separate, but related, standards IEEE Std 1164™-1993 [B16],[1] IEEE Std 1076.2™-1996 [B11], and IEEE Std 1076.3™-1997 [B12]; and general language enhancements in the areas of design and verification of electronic systems.

### 1.2 Purpose

The VHDL language was defined for use in the design and documentation of electronics systems. It is revised to incorporate capabilities that improve the language's usefulness for its intended purpose as well as extend it to address design verification methodologies that have developed in industry. These new design and verification capabilities are required to ensure VHDL remains relevant and valuable for use in electronic systems design and verification. Incorporation of previously separate, but related standards, simplifies the maintenance of the specifications.

[1]The numbers in brackets correspond to those of the bibliography in Annex J.