IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture

IEEE Computer Society

Sponsored by the
Test Technology Standards Committee

1149.7™

IEEE
3 Park Avenue
New York, NY 10016-5997, USA

10 February 2010

IEEE Std 1149.7™-2009

IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture

Sponsor

Test Technology Standards Committee

of the

IEEE Computer Society

Approved 9 December 2009

IEEE-SA Standards Board

Abstract: This specification describes circuitry that may be added to an integrated circuit to provide access to on-chip Test Access Ports (TAPs) specified by IEEE Std 1149.1™-2001. The circuitry uses IEEE 1149.1-2001 as its foundation, providing complete backward compatibility, while aggressively adding features to support test and applications debug. It defines six classes of 1149.7 Test Access Ports (TAP.7s), T0–T5, with each class providing incremental capability, building on that of the lower level classes. Class T0 provides the behavior specified by 1149.1 from startup when there are multiple on-chip TAPs. Class T1 adds common debug functions and features to minimize power consumption. Class T2 adds operating modes that maximize scan performance. It also provides an optional hot-connection capability to prevent system corruption when a connection is made to a powered system. Class T3 supports operation in either a four-wire Series or Star Scan Topology. Class T4 provides for communication with either a two-pin or four-pin interface. The two-pin operation serializes 1149.1 transactions and provides for higher Test Clock rates. Class T5 adds the ability to perform data transfers concurrent with scan, supports utilization of functions other than scan, and provides control of TAP.7 pins to custom debug technologies in a manner that ensures current and future interoperability.

Keywords: 1149.1, 1149.7, 2-pin, 2-wire, 4-pin, 4-wire, Advanced Protocol, Advanced Protocol Unit, APU, Background Data Transfer, background data transport, BDX, boundary scan, BSDL, BSDL.1, BSDL.7, BYPASS, Capture-IR, CDX, Chip-Level TAP Controller, CID, Class T0, Class T1, Class T2, Class T3, Class T4, Class T5, CLTAPC, compact JTAG, compliant behavior, compliant operation, control level, controller address, Controller ID, Controller Identification Number, CP, Custom Data Transfer, custom data transport, Data Register, debug interface, debug logic, debug and test interface, DOT1, DOT7, DTI, DTS, DTT, Debug Test System, debug test target, Escape, EOT, EPU, extended operation, Extended Protocol, EXTEST, HSDL, HSDL.7, IDCODE, Instruction Register, JScan, JScan0, JScan1, JScan2, JScan3, JTAG, MScan, MTCP, Multi-TAP Control Path, narrow Star Scan Topology, nTRST, nTRST_PD, optimized scan, OScan, OScan0, OScan1, OScan2, OScan3, OScan4, OScan5, OScan6, OScan7, 1149.1, 1149.7, Pause-DR, Pause-IR, PC0, PC1, RSU, Reset and selection unit, RTI, Run-Test/Idle, scan, scan DR, scan format, scan IR, Scan Packet, scan path, scan performance, scan protocol, scan topology, series, Series Branch, Series Scan, Series Scan Topology, Series-Equivalent Scan, Series Topology, Shift-DR, Shift-IR, SiP, Star Scan, Star Scan Topology, Star Topology, Star-2, Star-2 Branch, Star-2 Scan, Star-2, Scan Topology, Star-4, Star-4 Branch, Star-4 Scan, Star-4 Scan Topology, SP, SScan, SScan0, SScan1, SScan2, SScan3, stall, SSD, Scan Selection Directive, Standard Protocol, star scan, STL, System Test Logic, TAP, TAP controller, TAP controller address, TAP selection, TAP.1, TAP.7, TAP.7, TAPC, TCA, TCKC, TDI, TDIC, TDOC, TDOE, Test Access Port, test and debug, Test-Logic-Reset, TLR, TMSC, Transport Packet, T0, T0 TAP.7, T1, T1 TAP.7, T2, T2 TAP.7, T3, T3 TAP.7, T4, T4 TAP.7, T4(N), T4(N) TAP.7, T4(W), T4(W) TAP.7, T5, T5 TAP.7, T5(N), T5(N) TAP.7, T5(W), T5(W) TAP.7, TP, Update-DR, Update-IR, ZBS, zero bit scan

---

The Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue, New York, NY 10016-5997, USA

PDF: STD96012 978-0-7381-6153-2 STDCD96012 978-0-7381-6154-9

IEEE Standards documents are developed within the IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (IEEE-SA) Standards Board. The IEEE develops its standards through a consensus development process, approved by the American National Standards Institute, which brings together volunteers representing varied viewpoints and interests to achieve the final product. Volunteers are not necessarily members of the Institute and serve without compensation. While the IEEE administers the process and establishes rules to promote fairness in the consensus development process, the IEEE does not independently evaluate, test, or verify the accuracy of any of the information or the soundness of any judgments contained in its standards.

Use of an IEEE Standard is wholly voluntary. The IEEE disclaims liability for any personal injury, property or other damage, of any nature whatsoever, whether special, indirect, consequential, or compensatory, directly or indirectly resulting from the publication, use of, or reliance upon this, or any other IEEE Standard document.

The IEEE does not warrant or represent the accuracy or content of the material contained herein, and expressly disclaims any express or implied warranty, including any implied warranty of merchantability or fitness for a specific purpose, or that the use of the material contained herein is free from patent infringement. IEEE Standards documents are supplied "**AS IS**."

The existence of an IEEE Standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE Standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard. Every IEEE Standard is subjected to review at least every five years for revision or reaffirmation. When a document is more than five years old and has not been reaffirmed, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE Standard.

In publishing and making this document available, the IEEE is not suggesting or rendering professional or other services for, or on behalf of, any person or entity. Nor is the IEEE undertaking to perform any duty owed by any other person or entity to another. Any person utilizing this, and any other IEEE Standards document, should rely upon his or her independent judgment in the exercise of reasonable care in any given circumstances or, as appropriate, seek the advice of a competent professional in determining the appropriateness of a given IEEE standard.

Interpretations: Occasionally questions may arise regarding the meaning of portions of standards as they relate to specific applications. When the need for interpretations is brought to the attention of IEEE, the Institute will initiate action to prepare appropriate responses. Since IEEE Standards represent a consensus of concerned interests, it is important to ensure that any interpretation has also received the concurrence of a balance of interests. For this reason, IEEE and the members of its societies and Standards Coordinating Committees are not able to provide an instant response to interpretation requests except in those cases where the matter has previously received formal consideration. A statement, written or oral, that is not processed in accordance with the IEEE-SA Standards Board Operations Manual shall not be considered the official position of IEEE or any of its committees and shall not be considered to be, nor be relied upon as, a formal interpretation of the IEEE. At lectures, symposia, seminars, or educational courses, an individual presenting information on IEEE standards shall make it clear that his or her views should be considered the personal views of that individual rather than the formal position, explanation, or interpretation of the IEEE.

Comments for revision of IEEE Standards are welcome from any interested party, regardless of membership affiliation with IEEE. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Comments on standards and requests for interpretations should be submitted to the following address:

Secretary, IEEE-SA Standards Board
445 Hoes Lane
Piscataway, NJ 08854
USA

Introduction

This introduction is not part of IEEE Std 1149.7-2009, IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture.

This standard defines a debug and Test Access Port that provides both compatibility with IEEE Std 1149.1™-2001[a] and operation with as few as two pins. It complements IEEE Std 1149.1-2001 and is not intended to replace it. The facilities defined by the standard seek to provide a cost-effective debug and test interface solution supporting the debug and test of applications. The standard supports the needs for application debug of products with complex digital circuitry, applications software, and one or more central processing units (CPUs). The interface also provides a means to instrument these applications concurrent with scan transactions associated with the underlying IEEE 1149.1 foundation.

The process of developing this standard began in 2004 when the Mobile Industry Processor Interface (MIPI) Alliance Test and Debug Working Group was formed. During 2004, a standard that addressed the needs of both test and debug was described and requirements were gathered. The emphasis was on creating an interface that allowed standardization of access to debug and test capabilities on-chip while at the same time addressing the needs of applications developers sharing an integrated circuit's Test Access Port with test uses. This interface also targeted making chips exhibit the behavior that is specified by IEEE Std 1149.1-2001 when multiple Test Access Ports are deployed on a single chip. It was thought that applications development tools vendors would be a big beneficiary of this interface as common connectors providing access to the debug and test interface would be recommended. It was felt that all of this would best be accomplished with an interface that was compatible with chip intellectual property already utilizing IEEE Std 1149.1-2001.

Once the requirements gathering process was completed in 2004, the Test and Debug Working Group turned its attention to proposals for addressing the above requirements. Both competing and complementary proposals were submitted. The proposals were debated, and one was selected as a basis to move forward in April of 2005. A preliminary specification replaced the proposal and was reviewed inside the MIPI Test and Debug Working Group and by the NEXUS standards body in late 2005. Since both bodies felt the applicability of the specification was well beyond their own objectives, they both recommended using the on-chip portions of those specifications as the basis for an IEEE standard in a joint meeting in December of 2005.

Multiple drafts of the specification were completed and reviewed from 2005 until the standard's approval, with the capability provided by the standard expanded along the way. Revisions in the presentation and number of capabilities took place along the way to the standard's unanimous approval in 2009.

Notice to users

Laws and regulations

Users of these documents should consult all applicable laws and regulations. Compliance with the provisions of this standard does not imply compliance to any applicable regulatory requirements. Implementers of the standard are responsible for observing or referring to the applicable regulatory requirements. IEEE does not, by the publication of its standards, intend to urge action that is not in compliance with applicable laws, and these documents may not be construed as doing so.

[a] Information on references can be found in Clause 2.

Copyrights

Updating of IEEE documents

Users of IEEE standards should be aware that these documents may be superseded at any time by the issuance of new editions or may be amended from time to time through the issuance of amendments, corrigenda, or errata. An official IEEE document at any point in time consists of the current edition of the document together with any amendments, corrigenda, or errata then in effect. In order to determine whether a given document is the current edition and whether it has been amended through the issuance of amendments, corrigenda, or errata, visit the IEEE Standards Association Web site at http://ieeexplore.ieee.org/xpl/standards.jsp, or contact the IEEE at the address listed previously.

For more information about the IEEE Standards Association or the IEEE standards development process, visit the IEEE-SA Web site at http://standards.ieee.org.

Errata

Errata, if any, for this and all other standards can be accessed at the following URL: http://standards.ieee.org/reading/ieee/updates/errata/index.html. Users are encouraged to check this URL for errata periodically.

Interpretations

Current interpretations can be accessed at the following URL: http://standards.ieee.org/reading/ieee/interp/index.html.

Patents

Attention is called to the possibility that implementation of this recommended practice may require use of subject matter covered by patent rights. By publication of this recommended practice, no position is taken with respect to the existence or validity of any patent rights in connection therewith. The IEEE is not responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patents Claims or determining whether any licensing terms or conditions provided in connection with submission of a Letter of Assurance, if any, or in any licensing agreements are reasonable or non-discriminatory. Users of this recommended practice are expressly advised that determination of the validity of any patent rights, and the risk of infringement of such rights, is entirely their own responsibility. Further information may be obtained from the IEEE Standards Association.

Participants

At the time this standard was submitted to the IEEE-SA Standards Board for approval, the P1149.7 Working Group had the following membership:

Robert Oshana, *Chair*
Bart Vermeulen, *Vice Chair*
Gary Swoboda, *Technical Architect and Principal Author*

ARM Ltd.
ASSET InterTech, Inc.
Freescale Semiconductor
Intel Corporation
Lauterbach Datentechnik GmbH
Nokia Corporation
NXP Semiconductors
Texas Instruments

The following members of the entity balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

Alcatel-Lucent
ARM Ltd.
ASSET InterTech, Inc.
Freescale Semiconductor
IBM Corporation
Intel Corporation
Lauterbach Datentechnik GmbH
Nokia Corporation
NXP Semiconductors
Synopsys, Inc.
Texas Instruments

When the IEEE-SA Standards Board approved this standard on 9 December 2009, it had the following membership:

Robert M. Grow, *Chair*
Thomas Prevost, *Vice Chair*
Steve M. Mills, *Past Chair*
Judith Gorman, *Secretary*

John Barr
Karen Bartleson
Victor Berman
Ted Burse
Richard DeBlasio
Andy Drozd
Mark Epstein
Alexander Gelman
Jim Hughes
Richard H. Hulett
Young Kyun Kim
Joseph L. Koepfinger*
John Kulick
David J. Law
Ted Olsen
Glenn Parsons
Ronald C. Petersen
Narayanan Ramachandran
Jon Walter Rosdahl
Sam Sciacca

*Member Emeritus

Also included are the following nonvoting IEEE-SA Standards Board liaisons:

Howard L. Wolfman, *TAB Representative*
Michael Janezic, *NIST Representative*
Satish K. Aggarwal, *NRC Representative*

Don Messina
IEEE Standards Program Manager, Document Development

Michael D. Kipness
IEEE Standards Program Manager, Technical Program Development

Contents

1. Overview 1
1.1 Scope 1
1.2 Purpose 1
1.3 Contrasting IEEE Std 1149.1-2001 and this standard 2
1.4 Challenges 3
1.5 Important considerations 4
1.6 Nomenclature 4
1.6.1 References to technology and standards 4
1.6.2 Describing Test Access Port behaviors 4
1.6.3 Describing TAPs and TAP controllers 5
1.6.4 Describing scan exchanges 6
1.6.5 Describing TAP signals 6
1.7 Ensuring transparency to IEEE 1149.1 intellectual property 6
1.7.1 IEEE 1149.1 constraints 6
1.7.2 IEEE 1149.1 constraints/requirements balancing 7
1.7.3 IEEE 1149.1 upgrade path 7
1.8 Maximizing compatibility with 1149.1 IP 7
1.8.1 IEEE 1149.1 infrastructure 7
1.8.1.1 IEEE 1149.1 instructions 7
1.8.1.2 IEEE 1149.1 Scan Paths 8
1.8.1.3 IEEE 1149.1 boundary-scan capability 8
1.8.2 Test Clock treatment 8
1.8.2.1 Test Clock source 8
1.8.2.2 Test Clock shared or dedicated use 8
1.8.2.3 Unorthodox use of Test Clock 9
1.9 Scalability 10
1.9.1 Types of operation/capability classes 10
1.9.2 Signaling 11
1.10 Flexibility 12
1.10.1 Supporting various scan topologies 12
1.10.2 Operation with more than one scan topology/other technologies 13
1.11 Document content 14
1.11.1 Descriptive material 14
1.11.2 Specification material 15
1.12 Document organization 15
1.12.1 Partitioning 15
1.12.1.1 Foundation 16
1.12.1.2 TAP.7 Classes 17
1.12.1.3 Test description languages 17
1.12.1.4 Annexes 17
1.12.2 Pictorial view 18
1.13 Using the standard 19
1.13.1 User background knowledge 19
1.13.2 Types of users 19
1.13.2.1 Chip designer 19
1.13.2.2 Programmer 19
1.13.3 Use summary 19
1.14 Conventions 20
2. Normative references 26
3. Definitions, acronyms, and abbreviations 27
3.1 Definitions 27
3.2 Acronyms and abbreviations 31

4. TAP.7 concepts and architecture 36
4.1 Introduction 36
4.2 Concepts supporting system architecture 36
4.2.1 Maximizing compatibility with IEEE Std 1149.1-2001 36
4.2.1.1 Hardware components 37
4.2.1.2 Software components 37
4.2.2 TAPC hierarchy 37
4.2.2.1 Overview 37
4.2.2.2 Hierarchy levels 38
4.2.3 Parking the TAPC state 39
4.2.3.1 Overview 39
4.2.3.2 Parking-state relationships 40
4.2.3.3 Parking-state terminology 41
4.2.3.3.1 ADTAPC selection states 41
4.2.3.3.2 CLTAPC selection states 41
4.2.3.3.3 EMTAPC selection states 42
4.2.3.3.4 Selection state summary 43
4.2.4 Choice of parking states 43
4.2.5 Parking methods 43
4.2.6 Operation of the TAP.7 Controller 43
4.2.6.1 TAP.7 Controller management 43
4.2.6.2 System and Control Paths 44
4.2.6.3 Power management 45
4.2.7 Scan topologies 46
4.2.7.1 Series and Star Scan Topologies 46
4.2.7.2 Scan Topology Training 47
4.2.7.3 Sharing of signaling with other technologies 47
4.2.7.4 Direct addressability for Star Scan Topologies 47
4.2.7.5 Series-Equivalent Scans for Star Scan Topologies 48
4.2.7.6 Output-drive characteristics 49
4.2.7.7 Scan formats 50
4.2.7.8 Interoperability 51
4.3 Concepts supporting pin efficiency 51
4.3.1 Signaling methods 51
4.3.2 Protocols 52
4.3.2.1 Protocol types 52
4.3.2.2 Standard Protocol 53
4.3.2.3 Advanced Protocol 53
4.3.2.3.1 Interleaving of scan and non-scan information 54
4.3.2.3.2 Serialization of scan information 55
4.3.2.4 Control Protocol 56
4.3.3 Advanced and Control Protocol characteristics 56
4.3.3.1 Packets, bit-frames, and bits 56
4.3.3.2 Data and control information 57
4.3.4 Performance 58
4.3.4.1 TAP operation 58
4.3.4.1.1 Signal timing 58
4.3.4.1.2 Registering of signals 59
4.3.4.2 Scan transfer efficiency 59
4.4 Concepts supporting capability 59
4.4.1 Concepts already described 59
4.4.2 Resets 60
4.4.3 Private commands and registers 60
4.5 IEEE 1149.7 architecture 60
4.5.1 Components 60
4.5.2 Reset types 63

4.5.3 Start-up options ... 64
4.6 Operating models ... 65
4.6.1 Model types ... 65
4.6.2 Standard models ... 65
4.6.3 Advanced models ... 67
5. T0–T3 TAP.7 operational overview ... 68
5.1 Introduction ... 68
5.2 T0 TAP.7 ... 68
5.2.1 Overview ... 68
5.2.2 Operating modes and capabilities ... 69
5.2.3 Operation ... 70
5.2.3.1 Multi-TAPC architecture ... 70
5.2.3.2 Selection and deselection of EMTAPCs ... 70
5.2.4 T0 TAP.7 high-level block diagram ... 71
5.3 T1 TAP.7 ... 72
5.3.1 Overview ... 72
5.3.2 Operating modes and capabilities ... 73
5.3.3 Operation ... 73
5.3.3.1 Adding TAP.7 functionality to the *BYPASS* and *IDCODE* instructions ... 73
5.3.3.2 Zero-bit DR scans ... 73
5.3.3.3 Utilizing ZBSs for TAP.7 Controller functionality ... 74
5.3.3.3.1 Locking the ZBS count ... 74
5.3.3.3.2 Control levels ... 74
5.3.3.3.3 Exiting a control level ... 75
5.3.3.3.4 Zeroing the ZBS count ... 75
5.3.3.4 EPU Operating States ... 75
5.3.3.5 Commands ... 75
5.3.3.6 Registers ... 78
5.3.3.7 Using the System and Control Paths ... 80
5.3.3.7.1 System Path ... 81
5.3.3.7.2 Control Path ... 81
5.3.3.7.3 TDO Drive Policy ... 82
5.3.3.8 EPU groups ... 82
5.3.4 T1 TAP.7 high-level block diagram ... 82
5.4 T2 TAP.7 ... 82
5.4.1 Overview ... 82
5.4.2 Operating modes and capabilities ... 84
5.4.3 Operation ... 85
5.4.3.1 Overview ... 85
5.4.3.2 Using the System and Control Paths ... 86
5.4.3.3 TDO Drive Policy ... 87
5.4.3.4 STL groups ... 87
5.4.3.4.1 STL group types ... 87
5.4.3.4.2 STL Group Membership changes ... 88
5.4.4 T2 TAP.7 high-level block diagram ... 88
5.5 T3 TAP.7 ... 89
5.5.1 Overview ... 89
5.5.2 Operating modes and capabilities ... 90
5.5.3 Operation ... 92
5.5.3.1 Within series and star scan topologies ... 92
5.5.3.2 T3 TAP.7 Controller addressability in a Star-4 Scan Topology ... 92
5.5.3.3 Pause-IR and Pause-DR STL groups ... 92
5.5.3.4 Series/star scan equivalency ... 93
5.5.3.4.1 Defining scan equivalency ... 93
5.5.3.4.2 Creating a Series-Equivalent Scan within a Star Scan Topology ... 93

5.5.3.5 Scan Selection Directives 94
5.5.3.5.1 Enabling the use of SSDs 94
5.5.3.5.2 Types of SSDs 94
5.5.3.5.3 SSD execution 95
5.5.3.5.4 SSD State Machine 95
5.5.3.6 Series-Equivalent Scan creation 96
5.5.3.6.1 Exclusivity of SSD and TAP.7 Controller commands 97
5.5.3.7 Using the System and Control Paths 98
5.5.3.8 TDO Drive Policy 99
5.5.4 T3 TAP.7 high-level block diagram 99
6. T4–T5 TAP.7 operational overview 101
6.1 Introduction 101
6.2 T4 TAP.7 102
6.2.1 Operating modes and capabilities 102
6.2.2 Operation 103
6.2.2.1 Signal behaviors 103
6.2.2.2 Rising and falling TMSC input sampling 103
6.2.2.3 Controller addressability in a Star-2 Scan Topology 104
6.2.2.4 RSU and APU functions 104
6.2.2.4.1 Bypass (*BPA*) 106
6.2.2.4.2 Check Process Active (*CPA*) 106
6.2.2.4.3 Scan Packet Active (*SPA*) 109
6.2.3 T4 TAP.7 high-level block diagram 110
6.3 T5 TAP.7 111
6.3.1 Overview 111
6.3.2 Operating modes and capabilities 113
6.3.2.1 Transport source/destinations 113
6.3.2.1.1 Single-client operation 113
6.3.2.1.2 Multi-client operation 114
6.3.2.1.3 Client-to-client operation 115
6.3.2.2 Transfer characteristics 116
6.3.3 Operation 117
6.3.3.1 Transport Control Function 117
6.3.3.2 *TPA* 118
6.3.4 T5 TAP.7 high-level block diagram 119
6.4 TAP.7 feature summary 120
7. System concepts 122
7.1 Introduction 122
7.2 Key system attributes 122
7.3 DTS/TS connectivity with a mix of technologies 122
7.3.1 Technology mixes 122
7.3.2 Technology branches 123
7.4 TAP.7 deployment scenarios 124
7.4.1 TAP.1 Series Branches 124
7.4.2 TAP.7 Series, Star-4, and Star-2 Branches 124
7.5 Chip TAPC hierarchy 125
7.6 Combined view of TAP connectivity and TAPC hierarchy 126
7.7 Chips, components, and boards 127
8. TAPC hierarchy 129
8.1 Introduction 129
8.2 Selection/deselection with the TAPC hierarchy 129
8.2.1 Selection choices 129
8.2.2 Selection/deselection/class relationships 130
8.2.3 TAPC parent/child relationships 130
8.3 TAPC selection/deselection characteristics 130
8.3.1 TAPC and scan path behavior 130

8.3.2 Selection/deselection mechanisms 131
8.3.3 Parking states and resynchronization 131
8.4 ADTAPC selection/deselection 132
8.4.1 Parking use cases 132
8.4.2 DTS/ADTAPC relationship 132
8.4.3 ADTAPC operation 133
8.5 CLTAPC selection/deselection 134
8.5.1 Parking use cases 134
8.5.2 ADTAPC/CLTAPC relationship 134
8.5.3 CLTAPC operation 134
8.6 EMTAPC selection/deselection 136
8.6.1 Parking use cases 136
8.6.2 CLTAPC/EMTAPC relationship 136
8.6.3 EMTAPC operation 136
8.7 Using a common selection/deselection protocol across technologies 137
8.8 RSU deployment 137
8.8.1 Use with new or existing IP 137
8.8.2 Using TAP pins for multiple functions 138
8.9 Using the TAPC hierarchy 138
8.9.1 Selection considerations 138
8.9.2 Start-up considerations 139
8.10 Test/debug applications and the TAPC hierarchy 139
8.10.1 Debug use of the TAPC hierarchy 139
8.10.2 Test use of the TAPC hierarchy 140
9. Registers, commands, and scan paths 142
9.1 Introduction 142
9.2 Command basics 142
9.3 Register portfolio 144
9.3.1 Description 144
9.3.1.1 Global and Local Registers 144
9.3.1.2 Register loads 144
9.3.1.3 Register reset values 145
9.3.2 Specifications 145
9.4 Command portfolio 147
9.4.1 Description 147
9.4.1.1 Command types 147
9.4.1.2 Store commands 147
9.4.1.3 Select commands 148
9.4.1.4 Scan commands 148
9.4.1.5 Enumerate commands 148
9.4.1.6 Private commands 148
9.4.1.7 Effects a TAP.7 Controller reset 148
9.4.2 Specifications 149
9.5 Representation of commands in examples 154
9.6 Global and Local Register programming with commands 154
9.7 Scan paths 155
9.7.1 Conceptual and physical views 155
9.7.1.1 Description 155
9.7.1.1.1 Path characteristics 155
9.7.1.1.2 Conceptual path selection 155
9.7.1.1.3 Physical path selection 156
9.7.1.2 Specifications 157
9.7.2 EPU Scan Paths and their selection 159
9.7.2.1 Description 159
9.7.2.2 Specifications 159

9.7.3 EPU Scan Path characteristics 160
9.7.3.1 Description 160
9.7.3.1.1 Scan-path continuity 160
9.7.3.1.2 EPU Bypass-Path characteristics 161
9.7.3.1.3 EPU Bit-Path characteristics 161
9.7.3.1.4 EPU String-Path characteristics 161
9.7.3.1.5 Enumerate-Path characteristics 164
9.7.3.1.6 Auxiliary Path 164
9.7.3.2 Specifications 164
9.8 Two-part commands 166
9.9 Three-part commands 166
9.9.1 SCNB Command characteristics 166
9.9.2 SCNS Command characteristics 167
9.9.3 CIDA Command characteristics 168
9.10 RDBACKx and CNFGx Registers 170
9.10.1 RDBACKx Registers 171
9.10.1.1 Description 171
9.10.1.2 Specifications 171
9.10.2 CNFGx Registers 172
9.10.2.1 Description 172
9.10.2.1.1 Overview 172
9.10.2.1.2 CNFG0 mandatory configuration information 173
9.10.2.1.3 CNFG0 optional configuration information 173
9.10.2.1.4 CNFG1 optional configuration information 174
9.10.2.1.5 CNFG2 and CNFG3 Registers 174
9.10.2.1.6 Determining the TAP type and class using configuration information 174
9.10.2.2 Specifications 174
9.11 An approach to implementing command processing and scan paths 176
10. RSU ancillary services 180
10.1 Introduction 180
10.2 Resets 180
10.2.1 Description 180
10.2.1.1 Overview 180
10.2.1.2 Reset considerations 181
10.2.1.3 Reset effects 181
10.2.1.3.1 Type-5 Reset 182
10.2.1.3.2 Type-4 Reset 182
10.2.1.3.3 Type-3 Reset 182
10.2.1.3.4 Type-2 Reset 183
10.2.1.3.5 Type-1 Reset 183
10.2.1.3.6 Type-0 Reset 183
10.2.1.3.7 Type-0 versus a Type-2 Reset 183
10.2.1.4 TAP.7 Controller operation is ensured after power-up 183
10.2.1.5 Other effects of a TAP.7 Controller reset 183
10.2.1.6 An approach to implementing TAP.7 Controller resets 184
10.2.2 Specifications 185
10.3 Start-up options 187
10.3.1 Description 187
10.3.1.1 Overview 187
10.3.1.2 1149.1-compliant behavior start-up option 188
10.3.1.3 1149.1-Compatible Start-up option 188
10.3.1.4 IEEE 1149.1-Protocol Compatible 189
10.3.1.5 Offline-at-Start-up option 189
10.3.1.6 Start-up behavior 190
10.3.2 Specifications 191

10.4 Escape Detection 195
10.4.1 Description 195
10.4.1.1 Overview 195
10.4.1.2 Detection 196
10.4.1.2.1 Custom Escape 197
10.4.1.2.2 Selection and Deselection Escapes 197
10.4.1.3 Reset Escape 198
10.4.1.4 Timing considerations 198
10.4.1.5 An approach to implementing Escape Detection 198
10.4.2 Specifications 200
10.5 Selection Alert 201
10.5.1 Description 201
10.5.1.1 Overview 201
10.5.1.2 Selection Alert Bit Sequence 202
10.5.1.3 Selection Alert detection 203
10.5.1.4 An approach to implementing Selection Alerts 203
10.5.2 Specifications 205
10.6 Deselection Alert 207
10.6.1 Description 207
10.6.2 Specifications 207
10.7 Programming considerations 208
10.7.1 Resets 208
10.7.2 Escapes 208
10.7.3 Selection Alerts 208
10.7.4 Test and debug 208
10.7.5 Concurrent use of a Selection Escape and Selection Alert 208
10.8 ADTAPC State Machine 209
10.8.1 Need 209
10.8.2 An approach to implementing the ADTAPC 209
11. RSU Online/Offline capability 211
11.1 Introduction 211
11.2 Managing Online/Offline operation 211
11.3 Online/Offline operating principles 212
11.3.1 Conceptual view of Online/Offline operation 212
11.3.2 Events affecting Online/Offline operation 213
11.3.3 Summary of responses to selection/deselection events 214
11.3.4 Interoperability with other technologies 214
11.4 Initiating Offline operation 215
11.4.1 Description 215
11.4.1.1 Events initiating Offline operation 215
11.4.1.2 Escapes 216
11.4.1.3 Alerts 216
11.4.1.4 Use of an unsupported feature 217
11.4.1.5 Offline-at-Start-up 217
11.4.2 Specifications 217
11.5 Initiating Online operation 217
11.5.1 Description 217
11.5.2 Specifications 218
11.6 Context-sensitive response to Selection and Deselection Escapes 218
11.6.1 Description 218
11.6.1.1 Escape qualification criteria during Online operation 219
11.6.1.2 Escape qualification criteria during Offline-at-Start-up operation 219
11.6.1.3 Selection Alert during Offline-at-Start-up operation 220
11.6.2 Specifications 220
11.7 Selection Sequence 221
11.7.1 Initiation 221

11.7.2 Format 221
11.7.3 Technology-independent portion 221
11.7.4 Technology-dependent portion 222
11.7.5 Forms of Selection Sequence 222
11.7.6 Online Activation Code 223
11.7.6.1 Description 223
11.7.6.2 Specifications 224
11.7.7 TAP.7 Extension Code 227
11.7.7.1 Description 227
11.7.7.2 Specifications 227
11.7.8 Global Register load 229
11.7.8.1 Description 229
11.7.8.2 Specifications 230
11.7.9 Check Packet 230
11.7.9.1 Description 230
11.7.9.1.1 Format 230
11.7.9.1.2 Function 231
11.7.9.1.3 Directives 232
11.7.9.2 Specifications 232
11.8 Parking-state considerations 232
11.8.1 Description 232
11.8.2 Specifications 233
11.9 Control State Machine 235
11.9.1 Mandatory and optional behaviors 235
11.9.1.1 Description 235
11.9.1.2 Specifications 236
11.9.2 Standard state (*STD*) 237
11.9.2.1 Description 237
11.9.2.2 Specifications 237
11.9.3 Advanced state (*ADV*) 238
11.9.3.1 Description 238
11.9.3.2 Specifications 238
11.9.4 Offline waiting state (*OLW*) 239
11.9.4.1 Description 239
11.9.4.2 Specifications 239
11.9.5 Test state (*TEST*) 240
11.9.5.1 Description 240
11.9.5.1.1 Selection test 240
11.9.5.1.2 Factors requiring a Global Register load for placement Online 241
11.9.5.1.3 ADTAPC resynchronization 241
11.9.5.1.4 Priority of conditions causing state changes 242
11.9.5.1.5 Test state function 242
11.9.5.1.6 Selection Sequences requiring a state load 243
11.9.5.2 Specifications 244
11.9.6 Check Packet state (*CHK*) 247
11.9.6.1 Description 247
11.9.6.1.1 *CHK* substates 247
11.9.6.1.2 CP examples 248
11.9.6.2 Specifications 250
11.9.7 Offline-at-Start-up state (*OLS*) 253
11.9.7.1 Description 253
11.9.7.1.1 Placement Online 253
11.9.7.1.2 CLTAPC state initialization 253
11.9.7.1.3 Selection Escape qualification in the *OLS* state 253
11.9.7.1.4 Example of exiting the *OLS* state 254
11.9.7.2 Specifications 255

11.9.7.3 An approach to implementing the CSM 256
11.10 Programming considerations 258
11.10.1 Escapes 258
11.10.1.1 Selection Escape 258
11.10.1.2 Deselection Escape 258
11.10.1.3 Reset Escape 259
11.10.2 Alerts 259
11.10.2.1 Deselection Alert 259
11.10.2.2 Selection Alert 259
11.10.2.3 Offline-at-Start-up 259
11.10.3 Selection Sequences 260
11.10.3.1 DTS/TAP.7 Controller synchronization 260
11.10.3.2 Short Form 260
11.10.3.3 Long Form 260
11.10.4 Hang caused by a programming error 261
12. TAP signals 262
12.1 Introduction 262
12.2 TAP.7 Class/signal relationships 262
12.2.1 Description 262
12.2.2 Specifications 263
12.3 Signal function and bias 264
12.3.1 Description 264
12.3.2 Specifications 265
12.4 Test Reset (nTRST and nTRST_PD) signals 266
12.4.1 Description 266
12.4.2 Specifications 267
12.5 TAP.7 signal functions with corresponding IEEE 1149.1 names 267
12.5.1 Description 267
12.5.2 Specifications 267
12.6 Test Clock (TCK) 267
12.6.1 Description 267
12.6.2 Specifications 267
12.7 Test Mode Select (TMS/TMSC) 268
12.7.1 Description 268
12.7.1.1 Online start-up 268
12.7.1.2 Offline start-up 269
12.7.1.3 Combined view of Online and Offline-at-Start-up TMS(C) signal behaviors 271
12.7.2 Specifications 274
12.8 Test Data Input (TDI/TDIC) 275
12.8.1 Description 275
12.8.2 Specifications 276
12.9 Test Data Output (TDO/TDOC) 278
12.9.1 Description 278
12.9.2 Specifications 279
12.10 Offline-at-Start-up behavior 280
12.10.1 Description 280
12.10.2 Specifications 281
12.11 TAP connections 281
12.11.1 Description 281
12.11.2 Specifications 281
12.12 Applicability of this standard 282
12.12.1 Description 282
12.12.2 Specifications 282
12.13 Recommendations for interoperability 283
12.13.1 Overview 283
12.13.2 Power-up behavior 283

12.13.3 IEEE 1149.7-Non-disruptive behavior ... 283
12.13.3.1 Description ... 283
12.13.3.2 Specifications ... 284
12.13.4 IEEE 1149.7-Other Behavior ... 284
12.13.4.1 Description ... 284
12.13.4.2 Specifications ... 284
13. TDO(C) Signal Drive Policy ... 286
13.1 Introduction ... 286
13.2 TDO(C) Signal Drive Types ... 286
13.2.1 TDO(C) Signal Drive Types ... 286
13.2.1.1 Single Drive ... 287
13.2.1.2 Joint Drive ... 287
13.2.1.3 Voting Drive ... 287
13.2.1.4 Inhibited Drive ... 287
13.2.2 Wire-ANDed TDOC data created with a combination of drives ... 287
13.3 Factors affecting the TDO(C) Drive Policy ... 288
13.4 TDO(C) Drive Policy template ... 289
13.4.1 General characteristics ... 289
13.4.2 TDOC drive enables ... 289
13.4.3 TDO(C) Drive Policy components ... 289
13.4.4 TAP.7 Class/TDO(C) Drive Policy component applicability ... 290
13.4.5 Dormant TDO(C) Drive Policy ... 290
13.4.6 Transition TDO(C) Drive Policy ... 290
13.4.7 Series TDO(C) Drive Policy components ... 290
13.4.7.1 Series System ... 290
13.4.7.2 Series Command ... 291
13.4.7.3 Series Control Level ... 291
13.4.8 Star-4 TDO(C) Drive Policies ... 291
13.4.8.1 Star-4 System ... 291
13.4.8.2 Star-4 Command ... 291
13.4.8.3 Star-4 control level ... 292
13.4.9 Hierarchical and flat views of the TDO(C) Drive Policy ... 292
13.4.10 Conceptual diagram of the TDO(C) Drive Policy ... 295
13.5 T0 TAP.7 TDOC Drive Policy ... 296
13.5.1 Description ... 296
13.5.2 Specifications ... 296
13.6 T1 and T2 TAP.7 TDOC Drive Policy ... 297
13.6.1 Description ... 297
13.6.2 Specifications ... 298
13.7 T3 and above TAP.7 TDOC Drive Policy ... 299
13.7.1 Description ... 299
13.7.2 Specifications ... 300
13.8 STL Group Membership ... 302
13.8.1 Tracking the Group Membership of STLs ... 302
13.8.2 STL Group Membership changes ... 302
13.8.2.1 Group membership changes with the *Test-Logic-Reset* state ... 302
13.8.2.2 Group membership changes with the *Run-Test/Idle* state ... 302
13.8.2.3 Group membership changes with the *Pause-IR* state ... 303
13.8.2.4 Group membership changes with the *Pause-DR* state ... 303
13.8.3 Commands/SSDs affecting group Scan Group Candidacy and Membership ... 303
13.8.3.1 Commands affecting Scan Group Candidacy ... 303
13.8.3.2 SSDs affecting Scan Group Candidacy and Membership ... 304
13.8.3.2.1 SSDs associated with the *Run-Test/Idle* state ... 304
13.8.3.2.2 SSDs associated with the *Pause-IR* state ... 304
13.8.3.2.3 SSDs associated with the *Pause-DR* state ... 304

13.8.4 Only Scan Group Member determination 305
13.8.4.1 Criteria 305
13.8.4.2 Method and information used to make determination 305
13.8.4.2.1 Idle Group Membership and membership counts 305
13.8.4.2.2 Pause-xR Group Membership and membership counts 306
13.8.4.2.3 Scan Group Membership and membership counts 306
13.8.4.2.4 Information recorded 307
13.8.5 STL group candidate and membership counts 307
13.8.5.1 Description 307
13.8.5.1.1 Scan Group Candidate Count (SGCC) 307
13.8.5.1.2 Potential Scan Group Membership Count Last 309
13.8.5.1.3 Factors creating SGCC and PSGMCL ambiguity 310
13.8.5.2 Specifications 310
13.8.6 Scan Group Membership Count Last determination 313
13.8.6.1 Description 313
13.8.6.2 Specification 313
13.8.7 Only Scan Group Member Last determination 314
13.8.7.1 Description 314
13.8.7.2 Specification 314
13.9 EPU Group Membership 316
13.9.1 Description 316
13.9.1.1 Tracking the EPU's Group Membership 316
13.9.1.2 Conditional Group Member Count 316
13.9.1.3 Only Conditional Group Member determination 317
13.9.2 Specifications 318
13.10 Drive Policy summary 320
13.11 An approach to implementing TDOC Drive Policy 321
13.11.1 Policy generation 321
13.11.2 Potential Scan Group Member Last 322
13.11.3 The SGCC and PSGMCL functions 322
13.11.4 Determining Scan Group Only Member Last/Membership Count Last 323
13.11.5 The CGMC function 324
13.12 Programming considerations 324
14. TMS(C) Signal Drive Policy 325
14.1 Introduction 325
14.2 TMS(C) output bit types 325
14.2.1 Scan Packet content 325
14.2.2 Transport Packet content 326
14.2.3 Drive relationship with TCKC 327
14.3 Drive policy by output bit type 328
14.4 TMSC Signal Drive Types 329
14.4.1 TMSC Signal Drive Types 329
14.4.1.1 Single Drive 330
14.4.1.2 Joint Drive 330
14.4.1.3 Voting Drive 330
14.4.1.4 Inhibited Drive 330
14.4.2 Wire-ANDed TMSC signal values 330
14.5 Dormant Bit Drive Policy 331
14.5.1 Description 331
14.5.2 Specifications 331
14.6 Precharge Bit Drive Policy 331
14.6.1 Description 331
14.6.2 Specifications 331

14.7 RDY Bit Drive Policy 332
14.7.1 Description 332
14.7.1.1 Characteristics 332
14.7.1.2 Policy details 332
14.7.1.3 Relationship to CLTAPC selection state changes 333
14.7.2 Specifications 333
14.8 TDO Bit Drive Policy 335
14.8.1 Description 335
14.8.1.1 Characteristics 335
14.8.1.1.1 Policy details for System Path 335
14.8.1.1.2 Policy details for Control Path 336
14.8.1.2 Correlation to TDO(C) Drive Policy 336
14.8.1.3 Combined TDO bit drive summary 337
14.8.2 Specifications 338
14.9 Transport Bit Drive Policy 339
14.9.1 Description 339
14.9.2 Specifications 340
14.10 An approach to implementing TMSC Drive Policy 340
14.11 Programming considerations 344
15. IEEE 1149.1-compliance concepts 346
15.1 Introduction 346
15.2 Background 346
15.3 Test and debug views of a system of interest 347
15.4 An approach to implementing EMTAPC selection/deselection 348
16. T0 TAP.7 349
16.1 Introduction 349
16.2 Deployment 349
16.3 Capabilities 350
16.4 Configurations 350
16.4.1 Description 350
16.4.2 Specifications 350
16.5 Start-up behavior 351
16.5.1 Description 351
16.5.2 Specifications 351
16.6 Supporting multiple on-chip TAPCs 351
16.7 Controlling the selection state of EMTAPCs 352
16.7.1 Description 352
16.7.2 Specifications 353
16.8 Control via the CLTAPC Instruction Register 355
16.8.1 Description 355
16.8.1.1 Exclusion of TAPCs 355
16.8.1.2 Isolation of TAPCs 357
16.8.1.3 CLTAPC output registering of MTCP and MTDP control 358
16.8.2 Specifications 359
16.9 Control via one or more CLTAPC Data Registers 359
16.9.1 Description 359
16.9.2 Specifications 360
16.10 Control via internal or external *tapc_select* signals 361
16.10.1 Description 361
16.10.2 Specifications 362
16.11 Example use cases 363
16.11.1 IR control method with exclusions of TAPCs 364
16.11.2 IR control method with isolation of TAPCs 364
16.11.3 DR control method with exclusion of TAPCs 365

16.11.4 DR control method with isolation of TAPCs 365
16.12 Identification of on-chip TAP controller(s) 366
16.12.1 Description 366
16.12.2 Specifications 367
16.13 Multiple dies in one package 367
16.13.1 Description 367
16.13.1.1 Exposing an IEEE 1149.1 DR for the *BYPASS* and *IDCODE* instructions 368
16.13.1.2 Exposing the complete boundary-scan chain for IEEE 1149.1 instructions 368
16.13.1.3 BSDL documentation 368
16.13.1.4 Packaging dies 369
16.13.1.5 SiP-TAP POR* functionality 370
16.13.1.6 DR-wire bypass 370
16.13.2 Specifications 371
16.14 Managing STL Group Membership 372
16.15 RSU operation 372
16.15.1 Description 372
16.15.2 Specifications 372
16.16 Programming considerations 373
17. Extended concepts 374
17.1 Introduction 374
17.2 Suitability of *BYPASS* and *IDCODE* instructions for extended control 374
17.3 ZBS detection 374
17.3.1 Description 374
17.3.2 Specifications 375
17.4 Incrementing, locking, and clearing the ZBS count 375
17.4.1 Description 375
17.4.2 Specifications 376
17.5 Shared use of ZBSs by the EPU and STL 378
17.5.1 Description 378
17.5.1.1 EPU Operating States 378
17.5.1.2 EPU Operating State characteristics 379
17.5.1.3 ZBS use that is compatible with EPU Operating States 380
17.5.1.4 An approach to implementing EPU Operating States 381
17.5.2 Specifications 383
17.6 EPU functionality associated with the ZBS count 384
17.6.1 Description 384
17.6.2 Specifications 384
17.7 Programming considerations 385
18. T1 TAP.7 386
18.1 Introduction 386
18.2 Deployment 387
18.3 Capabilities 387
18.3.1 Inherited 387
18.3.2 New 388
18.4 Register and command portfolio 388
18.4.1 Description 388
18.4.1.1 General information 388
18.4.1.2 Register acronyms 389
18.4.1.3 Global Registers 390
18.4.1.4 Registers already described 390
18.4.1.5 New register descriptions 390
18.4.2 Specifications 390
18.5 Configurations 392
18.5.1 Description 392
18.5.2 Specifications 392

18.6 Start-up behavior 393
18.6.1 Description 393
18.6.2 Specifications 393
18.7 Conditional Group Membership 393
18.8 Test Reset 394
18.8.1 Description 394
18.8.2 Specifications 395
18.9 Functional reset 396
18.9.1 Description 396
18.9.2 Specifications 398
18.10 Power control 400
18.10.1 Description 400
18.10.1.1 Overview 400
18.10.1.1.1 Use cases 401
18.10.1.1.2 Power-control options 401
18.10.1.1.3 Power management within a typical system 402
18.10.1.1.4 Power-control topics 403
18.10.1.2 Power-Control Model 403
18.10.1.2.1 TAP.7 Controller power-management states 403
18.10.1.2.2 Key model attributes 404
18.10.1.3 The chip-level power manager's role in power control 405
18.10.1.3.1 Responsibilities 405
18.10.1.3.2 Interaction with TAP.7 Controller 405
18.10.1.3.3 Periods when a Type-0 Reset is asserted 406
18.10.1.3.4 Handling of power-up and power-down requests 406
18.10.1.3.5 Chip-Level power-up and power-down enables 407
18.10.1.3.6 The default Power-Control Mode 407
18.10.1.4 The DTS' role in power control 408
18.10.1.4.1 Responsibilities 408
18.10.1.4.2 Directed power-up 408
18.10.1.4.3 Detected power-up 409
18.10.1.5 The TAP.7 Controller's role in power control 410
18.10.1.5.1 Responsibilities 410
18.10.1.5.2 Operation 410
18.10.1.5.3 Test periods 411
18.10.1.5.4 Power-up confirmation test 412
18.10.1.5.5 Power-down initiation test 412
18.10.1.5.6 Power-down request summary 413
18.10.1.5.7 Awaiting power-down with the TAP.7 Controller operation shutdown 413
18.10.1.6 Example power-down sequences 414
18.10.1.7 An approach to implementing power control 416
18.10.2 Specifications 416
18.11 RSU operation 421
18.11.1 Description 421
18.11.2 Specifications 422
18.12 Programming considerations 422
19. T2 TAP.7 423
19.1 Introduction 423
19.2 Deployment 425
19.3 Capabilities 425
19.3.1 Inherited 425
19.3.2 New 425
19.4 Register and command portfolio 426
19.4.1 Description 426
19.4.1.1 General information 426
19.4.1.2 Register acronyms 426

19.4.1.3 Effects of a Long-Form Selection Sequence 426
19.4.1.4 New register descriptions 426
19.4.2 Specifications 427
19.5 Configurations 428
19.5.1 Description 428
19.5.2 Specifications 428
19.6 Start-up behavior 428
19.6.1 Description 428
19.6.2 Specifications 428
19.7 Scan formats 429
19.7.1 Description 429
19.7.2 Specifications 429
19.8 STL Group Membership 429
19.8.1 Description 429
19.8.1.1 Factors affecting group membership 429
19.8.1.2 Reset effects 430
19.8.1.3 TAPC state effects 430
19.8.1.4 Control Path effects 430
19.8.1.5 Parked state/selection relationships 432
19.8.1.6 Concurrent CLTAPC and EMTAPC selection changes 433
19.8.1.7 An approach to implementing CLTAPC selection with the T2 Class 434
19.8.2 Specifications 436
19.9 RSU operation 438
19.9.1 Description 438
19.9.2 Specifications 438
19.10 Programming considerations 439
20. T3 TAP.7 440
20.1 Introduction 440
20.2 Deployment 442
20.3 Capabilities 443
20.3.1 Inherited 443
20.3.2 New 443
20.4 Register and command portfolio 443
20.4.1 Description 443
20.4.1.1 General information 443
20.4.1.2 Register acronyms 444
20.4.1.3 Effect of a Long-Form Selection Sequence 444
20.4.2 Specifications 444
20.5 Configurations 445
20.5.1 Description 445
20.5.2 Specifications 446
20.6 Start-up behavior 446
20.6.1 Description 446
20.6.2 Specifications 446
20.7 Scan formats 446
20.7.1 Description 446
20.7.2 Specifications 447
20.8 TAP.7 Controller Address (TCA) 447
20.8.1 Description 447
20.8.2 Specifications 448
20.9 Aliasing the TCA to a Controller ID 449
20.9.1 Description 449
20.9.1.1 CID Allocate Command (CIDA) 449
20.9.1.1.1 CID-allocation criteria 450
20.9.1.1.2 CID-allocation candidates 450
20.9.1.1.3 CID-allocation process 450

20.9.1.1.4 Directed CID Allocation ... 451
20.9.1.1.5 Undirected CID Allocation ... 451
20.9.1.2 External AT generation with the JScan3 Scan Format ... 451
20.9.1.3 CID-allocation examples ... 452
20.9.1.4 An approach to implementing CID allocation ... 453
20.9.2 Specifications ... 454
20.10 Scan Selection Directives ... 457
20.10.1 Description ... 457
20.10.1.1 Overview ... 457
20.10.1.2 SSD format ... 458
20.10.1.3 SSD effects on STL Group Membership ... 458
20.10.1.4 Enabling SSD processing ... 459
20.10.1.5 SSD processing ... 459
20.10.1.6 Conditional SSD execution ... 462
20.10.1.7 SSD interaction with other controller functions ... 462
20.10.1.8 SSD State Machine ... 462
20.10.1.9 SSD states allowing Scan Group Membership ... 464
20.10.1.9.1 Using SSDs to create Series and Star-Equivalent Scans ... 465
20.10.1.9.2 Examples of SSD use ... 465
20.10.1.10 An approach to implementing the SSD function ... 470
20.10.2 Specifications ... 472
20.11 Scan Topology Training Sequence ... 476
20.11.1 Description ... 476
20.11.1.1 Overview ... 476
20.11.1.2 Topology Register Function ... 476
20.11.1.3 Use cases ... 477
20.11.1.3.1 Operation with a single TAP.7 Branch ... 477
20.11.1.3.2 Operation with more than one TAP.7 Branch ... 478
20.11.1.4 Scan-path characteristics used to determine the scan topology ... 478
20.11.1.5 Scan Topology Training Command Sequence ... 479
20.11.1.5.1 Connectivity test ... 480
20.11.1.5.2 Continuity test ... 480
20.11.2 Specifications ... 481
20.12 Managing STL Group Membership ... 481
20.12.1 Description ... 481
20.12.1.1 Factors affecting group membership ... 481
20.12.1.2 An approach to implementing CLTAPC selection with T3 and above classes ... 481
20.12.2 Specifications ... 483
20.13 RSU operation ... 485
20.13.1 Description ... 485
20.13.2 Specifications ... 486
20.14 Programming considerations ... 486
21. Advanced concepts ... 487
21.1 Architecture ... 487
21.2 Advanced capabilities ... 488
21.2.1 Mandatory and optional capabilities ... 488
21.2.2 Online and Offline operation ... 489
21.2.3 Interoperability with T0–T3 TAP.7s ... 489
21.2.4 Interoperability with T4 and above TAP.7s ... 489
21.3 Comparing the Standard and Advanced Protocols ... 490
21.4 APU functions ... 490
21.4.1 Conceptual view ... 490
21.4.2 Bypass Function ... 491
21.4.3 Scan Function ... 492
21.4.4 Transport Function ... 493
21.4.5 Bypass/Scan/Control Function interactions ... 495

21.5 APU interfaces ... 495
21.5.1 TAP ... 495
21.5.2 EPU ... 496
21.5.3 DCC ... 496
21.6 APU function/Operating State relationships ... 498
21.6.1 Operating State/function relationships ... 498
21.6.2 APU Operating State changes ... 499
21.6.3 Example operating state sequences ... 500
21.7 TAPC state/packet relationships ... 502
21.7.1 TAPC state and packet sequence relationships ... 502
21.7.2 Constructing packet sequences ... 504
21.7.3 Packet combinations/TAPC state relationships ... 505
21.7.4 Scheduling of packets ... 505
21.8 User's and implementer's views of the Advanced Protocol ... 507
21.8.1 User's view ... 507
21.8.2 Implementer's view ... 508
21.9 An approach to implementing APU Operating State scheduling ... 508
21.10 Structure of the clauses describing T4 and above TAP.7s ... 510
22. APU Scan Packets ... 512
22.1 CPs ... 512
22.2 SPs ... 512
22.2.1 Conceptual view of an SP ... 512
22.2.2 SP format ... 513
22.2.3 SP content ... 514
22.2.3.1 Header Element content ... 514
22.2.3.2 Payload Element content ... 514
22.2.3.3 Delay Element content ... 515
22.2.4 Types of output bit-frame transactions ... 516
22.3 SPs that advance the TAPC state ... 517
22.4 TPs ... 518
22.4.1 Conceptual view of a TP ... 518
22.4.2 TP format ... 518
22.4.3 Content ... 520
22.5 APU state diagram ... 520
22.6 An approach to implementing packet scheduling ... 522
22.6.1 Pipelining and its effects ... 522
22.6.2 SP Element scheduling ... 522
22.6.3 TP Element scheduling ... 523
23. T4 TAP.7 ... 524
23.1 Introduction ... 524
23.2 Deployment ... 524
23.3 Capabilities ... 525
23.3.1 Inherited ... 525
23.3.2 New ... 525
23.4 Register and command portfolio ... 526
23.4.1 Description ... 526
23.4.1.1 General information ... 526
23.4.1.2 Register acronyms ... 526
23.4.1.3 Effect of a Long-Form Selection Sequence ... 526
23.4.1.4 New register descriptions ... 527
23.4.1.4.1 Auxiliary Pin Function Control (APFC) Register ... 527
23.4.1.4.2 Delay Control (DLYC) Register ... 527
23.4.1.4.3 Ready Control (RDYC) Register ... 527
23.4.1.4.4 Sample Using Rising Edge (SREDGE) Register ... 527
23.4.1.4.5 Scan Format (SCNFMT) Register ... 527
23.4.1.4.6 System Test Clock Duty Cycle (STCKDC) Register ... 527

23.4.2 Specifications ... 528
23.5 Configurations ... 530
23.5.1 Description ... 530
23.5.2 Specifications ... 530
23.6 Start-up behavior ... 531
23.6.1 Description ... 531
23.6.2 Specifications ... 532
23.7 Scan formats ... 532
23.7.1 Overview ... 532
23.7.2 Addition of optional scan formats ... 534
23.7.3 Influences on scan format definition ... 534
23.7.4 Performance and flexibility tradeoffs ... 534
23.7.5 Comparing the scan formats ... 535
23.7.5.1 MScan ... 535
23.7.5.2 OScan ... 535
23.7.5.3 SScan ... 536
23.8 Configuration Faults ... 536
23.8.1 Description ... 536
23.8.2 Specifications ... 537
23.9 Increasing STL performance ... 537
23.9.1 Description ... 537
23.9.2 Specifications ... 539
23.10 Auxiliary Pin Function Control ... 540
23.10.1 Description ... 540
23.10.2 Specifications ... 541
23.11 Sample Using Rising Edge ... 541
23.11.1 Description ... 541
23.11.2 Specifications ... 541
23.12 System and EPU TMS signal values ... 542
23.12.1 Description ... 542
23.12.2 Specifications ... 543
23.13 System and EPU TDI signal values ... 544
23.13.1 Description ... 544
23.13.2 Specifications ... 545
23.14 RDY bit values ... 546
23.14.1 Description ... 546
23.14.2 Specifications ... 547
23.15 TDO bit values ... 548
23.15.1 Description ... 548
23.15.2 Specifications ... 549
23.16 Advanced Protocol effects on the EPU/CLTAPC relationship ... 549
23.16.1 Description ... 549
23.16.2 Specifications ... 549
23.17 SSD detection ... 549
23.17.1 Description ... 549
23.17.2 Specifications ... 549
23.18 Programming considerations ... 550
23.19 An approach to implementing a TAP.7 Controller with maximum performance ... 550
24. MScan Scan Format ... 552
24.1 Capabilities ... 552
24.1.1 Primary purpose ... 552
24.1.2 Application types supported ... 552
24.1.3 Important characteristics ... 553
24.2 High-level operation ... 553
24.3 Scan Packet content ... 554
24.3.1 Description ... 554

24.3.2 Specifications 554
24.4 Payload Element 554
24.4.1 Description 554
24.4.1.1 Format 554
24.4.1.2 Relationship to EPU signals 555
24.4.1.3 RDY bits 556
24.4.2 Specification 558
24.5 Delay Element 559
24.5.1 Description 559
24.5.1.1 Format 559
24.5.1.2 Delay Element Directives 559
24.5.1.3 Uses 560
24.5.2 Specifications 560
24.6 Advancing the TAPC state 562
24.6.1 Description 562
24.6.2 Specifications 562
24.7 CID allocation 562
24.7.1 Description 562
24.7.2 Specifications 564
24.8 Increasing STL performance with the MScan Scan Format 564
24.9 An approach to implementing the MScan Scan Format 564
24.9.1 Payload State Machine 564
24.9.2 Ready State Machine 566
24.9.3 Delay State Machine 567
24.10 Where to find examples 568
25. OScan Scan Formats 569
25.1 Capabilities 569
25.1.1 Primary purpose 569
25.1.2 Application types supported 569
25.1.3 Important characteristics 570
25.2 High-level operation 570
25.3 Scan Packet content 571
25.3.1 Description 571
25.3.2 Specifications 571
25.4 Payload Element 572
25.4.1 Description 572
25.4.1.1 Format 572
25.4.1.2 Optimizations 573
25.4.1.3 Relationship to EPU signals 574
25.4.1.4 Input bit-frame 578
25.4.1.5 Drive types 578
25.4.1.6 RDY bits 579
25.4.2 Specifications 580
25.5 Delay Element 581
25.6 Advancing the TAPC state 582
25.6.1 Description 582
25.6.2 Specifications 584
25.7 CID allocation 584
25.7.1 Description 584
25.7.2 Specifications 584
25.8 Increasing STL performance with OScan Scan Formats 585
25.9 An approach to implementing OScan Scan Formats 585
25.9.1 Payload State Machine 585
25.9.2 Shift Progress flag 587
25.9.3 CSM and SSM activation 588
25.9.4 RDY State Machine 588

25.9.5 TAP advance ... 589
25.10 Where to find examples ... 589
26. SScan Scan Formats ... 590
26.1 Capabilities ... 590
26.1.1 Primary purpose ... 590
26.1.2 Application types supported ... 591
26.1.3 Control Segments ... 592
26.1.4 Data Segments ... 593
26.1.5 Stall profiles ... 593
26.1.6 Important characteristics ... 594
26.2 High-level operation ... 594
26.2.1 Overview ... 594
26.2.2 Segments and their use ... 595
26.2.2.1 Description ... 595
26.2.2.1.1 Use with a TAP.1-like component ... 595
26.2.2.1.2 Use with a DMA or FIFO component ... 596
26.2.2.1.3 Use with a direct-access data-rate-dependent component ... 597
26.2.2.1.4 Use with a buffered TDI/TMS component ... 597
26.2.2.1.5 Utilizing the same scan format for two applications types ... 598
26.2.2.2 Specifications ... 599
26.3 Scan Packet content ... 599
26.3.1 Description ... 599
26.3.2 Specifications ... 600
26.4 Header Element ... 601
26.4.1 Description ... 601
26.4.2 Specifications ... 601
26.5 Payload Element ... 602
26.5.1 Description ... 602
26.5.1.1 Factors determining payload content ... 602
26.5.1.2 Optimizations ... 604
26.5.1.3 Input bit-frame ... 607
26.5.1.4 Output bit-frame ... 610
26.5.1.4.1 Content ... 610
26.5.1.4.2 SScan0/1 output-only segments ... 610
26.5.1.4.3 SScan2/3 output-only segments ... 611
26.5.2 Specifications ... 615
26.6 Delay Element ... 617
26.7 Packet sequences and factors influencing them ... 618
26.7.1 Description ... 618
26.7.2 Specifications ... 621
26.8 Advancing the TAPC state ... 621
26.8.1 Description ... 621
26.8.1.1 SP followed by a CP ... 621
26.8.1.2 Control Segments ... 621
26.8.1.3 Data Segments ... 621
26.8.2 Specifications ... 626
26.9 CID allocation ... 626
26.9.1 Description ... 626
26.9.2 Specifications ... 626
26.10 Increasing STL performance with SScan Scan Formats ... 627
26.11 An approach to implementing SScan Scan Formats ... 627
26.11.1 Payload State Machine ... 627
26.11.2 Escape Detection State Machine ... 628
26.11.3 Shift Progress flag ... 629
26.11.4 TAP advance ... 630
26.11.5 Additional entry point loads for output-only segments ... 630

26.11.6 Header Register ... 631
26.11.7 Timing diagrams ... 632
26.12 Where to find examples ... 634
27. T5 TAP.7 ... 635
27.1 Introduction ... 635
27.2 Deployment ... 636
27.3 Capabilities ... 637
27.3.1 Inherited ... 637
27.3.2 New ... 637
27.4 Register and command portfolio ... 637
27.4.1 Description ... 637
27.4.1.1 General information ... 637
27.4.1.2 Register acronyms ... 638
27.4.1.3 Effect of a Long-Form Selection Sequence ... 638
27.4.1.4 Transport protocol revision (TPPREV) register ... 638
27.4.1.5 Transport states (TPST) ... 639
27.4.1.6 Data Element length (TP_DELN) ... 639
27.4.1.7 Physical Data Channel to Logical Data Channel association (PDCx_LCA) ... 639
27.4.1.8 Physical Data Channel selected (PDCx_SEL) ... 639
27.4.1.9 Physical Data Channel DCC selection (PDCx_DCC) ... 639
27.4.1.10 Physical Data Channel DCC Control Registers (PDCx_DCCy_CRz) ... 639
27.4.2 Specifications ... 640
27.5 Configurations ... 644
27.5.1 Description ... 644
27.5.2 Specifications ... 645
27.6 Start-up behavior ... 646
27.6.1 Description ... 646
27.6.2 Specifications ... 646
27.7 Configuration Faults ... 646
27.7.1 Description ... 646
27.7.2 Specifications ... 646
27.8 Enabling transport ... 647
27.8.1 Description ... 647
27.8.2 Specifications ... 647
27.9 Transport Packet composition ... 648
27.9.1 Operations ... 648
27.9.2 Directive, Register, and Data Elements ... 649
27.10 Directive Elements ... 649
27.10.1 Description ... 649
27.10.1.1 Overview ... 649
27.10.1.2 Directive Element acronyms ... 650
27.10.1.3 Surrounding context of directives ... 650
27.10.1.4 Directive/transport building block relationships ... 651
27.10.1.5 Directive encoding ... 652
27.10.1.6 Directive types ... 653
27.10.1.6.1 Unconditional Directives ... 654
27.10.1.6.2 Reset Directives ... 654
27.10.1.6.3 Selection Directives ... 654
27.10.1.6.4 Conditional Directives ... 655
27.10.1.6.5 Transfer Directives ... 656
27.10.2 Specifications ... 656
27.11 Register Elements ... 660
27.11.1 Description ... 660
27.11.1.1 Overview ... 660
27.11.1.2 Register Element length ... 660
27.11.1.3 Transfer direction ... 660

27.11.1.4 Summary of Register Element characteristics 660
27.11.2 Specifications 661
27.12 Data Elements 661
27.12.1 Description 661
27.12.1.1 Overview 661
27.12.1.2 Data Element length 661
27.12.1.3 Transfer direction 661
27.12.1.4 Utilization and generation of data 662
27.12.1.5 Operation with single and multiple clients 662
27.12.1.6 Summary of Data Element characteristics 663
27.12.2 Specifications 663
27.13 Selection of control and data targets 664
27.14 Data Channel Client functions 665
27.14.1 Description 665
27.14.1.1 Initializing a Data Channel Client 665
27.14.1.2 Orderly shutdown of a transfer 665
27.14.1.3 Effects of Online/Offline operation on the Transport Function 666
27.14.2 Specifications 667
27.15 Partitioning of the Transport Control Function 667
27.15.1 Building blocks 667
27.15.2 Directive/register/operational relationships 669
27.16 Programming considerations 670
27.16.1 Managing transport with the DTS 670
27.16.2 Single and multi-client data exchanges 670
27.16.3 Bandwidth allocation 670
27.16.4 Common and uncommon operations performed with directives 670
27.16.5 Dynamic source/destination changes 671
27.16.6 Transfer alignment characteristics 672
27.17 Aspects of transport not covered by this specification 672
28. Transport operation and interfaces 673
28.1 Introduction 673
28.2 TAP interface 673
28.2.1 *TPA* state flow 673
28.2.2 Directive Element characteristics 674
28.2.2.1 Description 674
28.2.2.2 Specifications 674
28.2.3 Register Element characteristics 676
28.2.3.1 Description 676
28.2.3.1.1 Format, timing, and TMSC signal drive characteristics 676
28.2.3.1.2 Register Element length 676
28.2.3.1.3 Register Element content 677
28.2.3.2 Specifications 678
28.2.4 Data Element characteristics 679
28.2.4.1 Description 679
28.2.4.1.1 Format, timing, and TMSC signal drive characteristics 679
28.2.4.1.2 Data Element length 680
28.2.4.1.3 Data Element content 681
28.2.4.1.4 Drive characteristics 682
28.2.4.1.5 Multi-client data transfers 682
28.2.4.1.6 Data Element alignment with the data that is transported 683
28.2.4.2 Specifications 683
28.3 Transport State Machine 684
28.3.1 Description 684
28.3.1.1 Conceptual view 684
28.3.1.2 TSM operation 686
28.3.1.3 Scheduling a TP 687

28.3.1.4 Starting/restarting directive processing 689
28.3.1.5 Completing a TP 689
28.3.2 Specifications 690
28.4 PDCx/DCC interface 691
28.4.1 Description 691
28.4.1.1 Signal functions 692
28.4.1.2 Signal descriptions 692
28.4.1.3 Signal use 694
28.4.2 Specifications 698
28.5 Five-bit directives 698
28.5.1 Description 698
28.5.2 Specifications 698
28.6 Eight-bit directives 701
28.6.1 Description 701
28.6.2 Specifications 701
28.7 12-bit directives 702
28.7.1 Description 702
28.7.2 Specifications 702
28.8 DCC interface operation 705
28.8.1 Basic capability 705
28.8.2 Pipelining register *dcc_rdo* signaling 706
28.8.3 Pipelining *dcc_ddo* and *dcc_cor* signaling 706
28.9 An approach to implementing the Transport Function 707
28.9.1 Overview 707
28.9.2 The Transport State Machine 708
28.9.3 Multi-use Register bits 709
28.9.3.1 Input configurations 709
28.9.3.2 Transport Packet processing 710
28.9.3.2.1 Directive processing 710
28.9.3.2.2 Data Element processing 710
28.9.3.2.3 12-bit directive processing (other than TP_CRR and TP_CRW) 711
28.9.3.2.4 TP_CRR and TP_CRW Directive processing 711
28.9.3.3 TSM state/register value relationships 712
28.9.3.4 Transport output and DCR input selection 715
28.9.3.5 TP activity examples 717
29. Test concepts 722
29.1 Introduction 722
29.2 Interoperability 722
29.3 Construction of the unit under test 723
29.4 Background (IEEE 1149.1 paradigm) 723
29.4.1 Topology 724
29.4.2 Scan-state sequencing 724
29.5 Implications for test applications arising from this standard 725
29.5.1 Divergences versus IEEE Std 1149.1-2001 725
29.5.2 Accommodation/resolution of divergences versus IEEE Std 1149.1-2001 726
29.6 Test example—a narrative 726
29.7 Describing the unit under test 727
29.8 Documentation model 728
29.9 Considerations for large-system applications 729
30. Documenting IEEE 1149.7 test endpoints (BSDL.7) 731
30.1 Introduction 731
30.2 Conventions 732
30.3 Purpose of BSDL.7 732
30.4 Scope of BSDL.7 732
30.5 Expectations of a BSDL.7 parser 733
30.6 Relationship of BSDL.7 to BSDL.1 733

30.6.1 Description ... 733
30.6.2 Specifications ... 734
30.7 Lexical elements of BSDL.7 ... 734
30.7.1 Description ... 734
30.7.2 Specifications ... 734
30.8 BSDL.7 reserved words ... 734
30.8.1 Description ... 734
30.8.2 Specifications ... 734
30.9 Components of a BSDL.7 description ... 735
30.9.1 Description ... 735
30.9.2 Specifications ... 735
30.10 The entity description (BSDL.7) ... 735
30.10.1 Overall structure of the entity description (BSDL.7) ... 735
30.10.1.1 Syntax and content ... 735
30.10.1.1.1 Description ... 735
30.10.1.1.2 Specifications ... 736
30.10.1.2 Semantic checks ... 737
30.10.1.2.1 Description ... 737
30.10.1.2.2 Specifications ... 737
30.10.2 Standard use statement (BSDL.7) ... 737
30.10.2.1 Syntax and content ... 737
30.10.2.1.1 Description ... 737
30.10.2.1.2 Specifications ... 737
30.10.2.2 Examples ... 738
30.10.3 Version control ... 739
30.10.3.1 Syntax and content ... 739
30.10.3.1.1 Description ... 739
30.10.3.1.2 Specifications ... 739
30.10.4 Component conformance statement (BSDL.7) ... 739
30.10.4.1 Syntax and content ... 739
30.10.4.1.1 Description ... 739
30.10.4.1.2 Specifications ... 739
30.10.4.2 Examples ... 740
30.10.4.3 Semantic checks ... 740
30.10.5 Scan port identification (BSDL.7) ... 740
30.10.5.1 Syntax and content ... 740
30.10.5.1.1 Description ... 740
30.10.5.1.2 Specifications ... 740
30.10.5.2 Examples ... 741
30.10.5.3 Semantic checks ... 742
30.10.5.3.1 Description ... 742
30.10.5.3.2 Specifications ... 743
30.10.6 Compliance enable description (BSDL.7) ... 744
30.10.6.1 Syntax and content ... 744
30.10.6.1.1 Description ... 744
30.10.6.1.2 Specifications ... 744
30.10.6.2 Examples ... 744
30.10.6.3 Semantic checks ... 744
30.10.6.3.1 Description ... 744
30.10.6.3.2 Specifications ... 745
30.10.7 Device identification register description (BSDL.7) ... 745
30.10.7.1 Syntax and content ... 745
30.10.7.1.1 Description ... 745
30.10.7.1.2 Specifications ... 745
30.10.7.2 Examples ... 745
30.10.7.3 Semantic checks ... 745

30.10.7.3.1 Description ... 745
30.10.7.3.2 Specifications ... 745
30.10.8 Configuration register description (BSDL.7) ... 746
30.10.8.1 Syntax and content ... 746
30.10.8.1.1 Description ... 746
30.10.8.1.2 Specifications ... 746
30.10.8.2 Examples ... 746
30.10.8.3 Semantic checks ... 747
30.10.8.3.1 Description ... 747
30.10.8.3.2 Specifications ... 747
30.11 The Standard VHDL Package STD_1149_7_2009 ... 747
30.11.1 Description ... 747
30.11.2 Specifications ... 747
30.12 A typical application of BSDL.7 ... 748
31. Documenting IEEE 1149.7 test modules (HSDL.7) ... 751
31.1 Introduction ... 751
31.2 Conventions ... 751
31.3 Purpose of HSDL.7 ... 752
31.4 Scope of HSDL.7 ... 752
31.5 Expectations of an HSDL.7 parser ... 753
31.6 Relationship of HSDL.7 to BSDL.7 (and BSDL.1) ... 753
31.6.1 Description ... 753
31.6.2 Specifications ... 754
31.7 Lexical elements of HSDL.7 ... 754
31.7.1 Description ... 754
31.7.2 Specifications ... 754
31.8 HSDL.7 reserved words ... 754
31.8.1 Description ... 754
31.8.2 Specifications ... 754
31.9 Components of an HSDL.7 description ... 754
31.9.1 Description ... 754
31.9.2 Specifications ... 755
31.10 The entity description (HSDL.7) ... 755
31.10.1 Overall structure of the entity description (HSDL.7) ... 755
31.10.1.1 Syntax and content ... 755
31.10.1.1.1 Description ... 755
31.10.1.1.2 Specifications ... 755
31.10.1.2 Semantic checks ... 756
31.10.1.2.1 Description ... 756
31.10.1.2.2 Specifications ... 756
31.10.2 Module standard use statement (HSDL.7) ... 756
31.10.2.1 Syntax and content ... 756
31.10.2.1.1 Description ... 756
31.10.2.1.2 Specifications ... 757
31.10.2.2 Examples ... 758
31.10.3 Version control ... 758
31.10.3.1 Syntax and content ... 758
31.10.3.1.1 Description ... 758
31.10.3.1.2 Specifications ... 758
31.10.4 Module component conformance statement (HSDL.7) ... 759
31.10.4.1 Syntax and content ... 759
31.10.4.1.1 Description ... 759
31.10.4.1.2 Specifications ... 759
31.10.4.2 Examples ... 759
31.10.4.3 Semantic checks ... 759

31.10.5 Module package pin mappings (HSDL.7) ... 760
31.10.5.1 Syntax and content ... 760
31.10.5.1.1 Description ... 760
31.10.5.1.2 Specifications ... 760
31.10.5.2 Examples ... 760
31.10.5.3 Semantic checks ... 760
31.10.5.3.1 Description ... 760
31.10.5.3.2 Specifications ... 760
31.10.6 Module scan port identification (HSDL.7) ... 760
31.10.6.1 Syntax and content ... 760
31.10.6.1.1 Description ... 760
31.10.6.1.2 Specifications ... 761
31.10.6.2 Examples ... 761
31.10.6.3 Semantic checks ... 762
31.10.6.3.1 Description ... 762
31.10.6.3.2 Specifications ... 762
31.10.7 Module members declaration (HSDL.7) ... 763
31.10.7.1 Syntax and content ... 763
31.10.7.1.1 Description ... 763
31.10.7.1.2 Specifications ... 764
31.10.7.2 Examples ... 765
31.10.7.3 Semantic checks ... 766
31.10.7.3.1 Description ... 766
31.10.7.3.2 Specifications ... 766
31.11 The Standard VHDL Package STD_1149_7_2009_module ... 767
31.11.1 Description ... 767
31.11.2 Specifications ... 767
31.12 Applications of HSDL.7 ... 767
31.12.1 HSDL.7 for Figure 4-1 of IEEE Std 1149.1-2001 ... 767
31.12.2 HSDL.7 for Figure 4-2 of IEEE Std 1149.1-2001 ... 769
31.12.3 HSDL.7 for a basic Star Scan Topology ... 770
31.12.4 HSDL.7 for a basic hierarchical topology ... 771
31.12.5 A typical application of HSDL.7 ... 773
Annex A (informative) IEEE 1149.1 reference material ... 775
Annex B (informative) Scan examples in timing diagram form ... 778
B.1 MScan and OScan SP types ... 778
B.2 MScan and OScan transactions ... 779
B.3 SScan transactions ... 789
B.4 BDX and CDX Transport Packet examples ... 803
Annex C (informative) Scan examples in tabular form ... 805
C.1 Overview ... 805
C.2 MScan and OScan SP types ... 805
C.3 SScan SP types ... 820
Annex D (informative) Programming considerations ... 847
D.1 Overview ... 847
D.2 DTS' view of TAPs ... 847
D.3 Scan topology interrogation ... 860
D.4 Establishing TAP.7 operating conditions ... 873
D.5 CID management ... 873
D.6 Managing simultaneous debug actions ... 874
D.7 Operations to avoid with a Star-4 Scan Topology ... 874
D.8 Using a T5 TAP.7 ... 875
Annex E (informative) Recommended electrical characteristics ... 876
Annex F (informative) Connectivity/electrical recommendations ... 877
F.1 Overview ... 877
F.2 Physical connection topologies considered ... 879

F.3 Termination schemes considered 880
F.4 Chip considerations 882
F.5 Board considerations 885
F.6 DTS considerations 903
F.7 Point-to-Point configuration 907
F.8 Line configuration of a transmission line 911
F.9 T configuration of a transmission line 929
F.10 X configuration of a transmission line 937
F.11 XT configuration of a transmission line 947
F.12 Recommendations 956
Annex G (informative) Utilizing SScan Scan Formats 962
Annex H (informative) The RTCK signal 966
Annex I (informative) Bibliography 974

Figures

Figure 1-1 — IEEE 1149.7 impact areas 2
Figure 1-2 — IEEE 1149.7/IEEE 1149.1 upgrade path 7
Figure 1-3 — Systems where the DTS and TS source the Test Clock 8
Figure 1-4 — Dedicated and Shared Test Clock signal 9
Figure 1-5 — Systems with a Return Test Clock 9
Figure 1-6 — Types of TAP.7 operation 10
Figure 1-7 — TAP.7 capability classes and their layered capability 11
Figure 1-8 — Utilization of TAP.7 Classes within scan topologies 12
Figure 1-9 — A system with TCK(C) and TMS(C) shared between TAP.7 and technologies 14
Figure 1-10 — IEEE 1149.7 standard organization 16
Figure 1-11 — Document organization 18
Figure 1-12 — Clause subject areas 20
Figure 1-13 — Annex subject areas 20
Figure 1-14 — Arc priority 24
Figure 1-15 — Flowchart symbol expansion 24
Figure 1-16 — MSB/LSB conventions 25
Figure 4-1 — Scan architectures utilizing IEEE Std 1149.1-2001 38
Figure 4-2 — TAP.7 TAPC hierarchy 39
Figure 4-3 — Relationships of parking the TAPC state to its associated resources 40
Figure 4-4 — TAP.7 Controller management 44
Figure 4-5 — System and Control Path relationship 45
Figure 4-6 — Components involved in TAP.7 Controller power management 46
Figure 4-7 — TAP.7 Protocols and Escapes 53
Figure 4-8 — Control/Standard/Advanced Protocol relationships 55
Figure 4-9 — Expanded view of an SP sequence with the OScan1 Scan Format 55
Figure 4-10 — Control Protocol/Standard and Advanced Protocol relationships 56
Figure 4-11 — Packets, bit-frames, and bits 57
Figure 4-12 — TAP.7 architecture 61
Figure 4-13 — Conceptual view of the interface bridge 62
Figure 4-14 — Operating model types 65
Figure 4-15 — Conceptual view of basic T0–T2 TAP.7 operation without RSU 66
Figure 4-16 — Conceptual view of T0–T3 TAP.7 operation with an RSU 66
Figure 4-17 — TMSC pin utilization flow diagram for a T5 TAP.7 67
Figure 5-1 — T0 TAP.7 chip block diagram 68
Figure 5-2 — T0 TAP.7 test and debug views of the chip 69
Figure 5-3 — System-on-Chip (SoC) with IEEE 1149.7 multiple TAPC architecture 70
Figure 5-4 — High-level T0 TAP.7 functional block diagram 72
Figure 5-5 — T1 TAP.7 chip block diagram 72
Figure 5-6 — T1 TAP.7 features 73
Figure 5-7 — Command generation 76
Figure 5-8 — DR-Scan sequence used for command creation 77
Figure 5-9 — High-level view of TAP.7 Controller registers 78
Figure 5-10 — High-level view of TAP.7 Controller Global/Local Registers 79
Figure 5-11 — T1 TAP.7 physical and conceptual path relationships 80
Figure 5-12 — T1 TAP.7 Control and System Paths 81
Figure 5-13 — High-level T1 TAP.7 functional block diagram 83
Figure 5-14 — T2 TAP.7 chip block diagram 83
Figure 5-15 — T2 TAP.7 scan-path length reduction 85
Figure 5-16 — T2 TAP.7 physical and conceptual path relationships 86
Figure 5-17 — T2 TAP.7 Control and System Paths 87
Figure 5-18 — T2 TAP.7 group membership determination 88

Figure 5-19 — High-level T2 TAP.7 functional block diagram 89
Figure 5-20 — T3 TAP.7 chip block diagram 90
Figure 5-21 — T3 TAP.7 scan-path length reduction 91
Figure 5-22 — T3 TAP.7 group membership related to the use of the System Path 93
Figure 5-23 — Series-Equivalent Scan using SSDs in a Star Scan Topology 97
Figure 5-24 — T2 TAP.7 physical and conceptual path relationships 98
Figure 5-25 — T2 TAP.7 Control and System Paths 99
Figure 5-26 — High-level T3 TAP.7 functional block diagram 100
Figure 6-1 — T4/T5 TAP.7 chip block diagram 101
Figure 6-2 — Conceptual block diagram of the functions of a T4 TAP.7 104
Figure 6-3 — TMSC pin utilization flow diagram for a T4 TAP.7 105
Figure 6-4 — *CPA* state entry from the *BPA* state with subsequent Online operation 106
Figure 6-5 — *CPA* state entry from the *SPA* state with subsequent Online operation 107
Figure 6-6 — *CPA* state entry from the *BPA* state with subsequent Offline operation 107
Figure 6-7 — *CPA* state entry from the *SPA* state with subsequent Offline operation 108
Figure 6-8 — Reset initiated *CPA* state entry/awaiting a Selection Sequence for an exit 108
Figure 6-9 — SP and TAPC state relationships 109
Figure 6-10 — Expanded view of an SP sequence 109
Figure 6-11 — Serialization and de-serialization of SP information 110
Figure 6-12 — High-level T4 TAP.7 functional block diagram 111
Figure 6-13 — T5 TAP.7 chip block diagram 112
Figure 6-14 — Logical channel configurations 113
Figure 6-15 — DTS data exchanges with one client 114
Figure 6-16 — DTS data exchanges with more than one client 115
Figure 6-17 — DTS data exchange between multiple clients 116
Figure 6-18 — Conceptual block diagram of the functions of T5 TAP.7 117
Figure 6-19 — TMSC pin utilization flow diagram for a T5 TAP.7 118
Figure 6-20 — TP placement and content 119
Figure 6-21 — High-level T5 TAP.7 functional block diagram 120
Figure 7-1 — System connectivity with mixed use of technologies and scan topologies 123
Figure 7-2 — TAP.1 Series Branches 124
Figure 7-3 — TAP.7 Series, Star-4, and Star-2 Scan Topologies 125
Figure 7-4 — TAP.7 TAPC hierarchy 126
Figure 7-5 — System connectivity supported by the TAP.7 architecture 127
Figure 7-6 — Contrasting IEEE 1149.1 and IEEE 1149.7 test views 128
Figure 8-1 — Parking the ADTAPC state 134
Figure 8-2 — Parking the Chip-Level TAPC state 135
Figure 8-3 — Parking the Chip-Level TAPC state 137
Figure 8-4 — Selection within a chip or system 138
Figure 8-5 — Example of debug use of the RSU 139
Figure 8-6 — Using Series/Star-4/and Star-2 Scan Topologies concurrently 140
Figure 9-1 — DR Scan sequence used for command creation 143
Figure 9-2 — Command completion timing 149
Figure 9-3 — Command construction and execution 150
Figure 9-4 — Conceptual to physical path mapping paths 156
Figure 9-5 — Conceptual view of the T1 and above TAP.7 Scan Paths 157
Figure 9-6 — Saved Scan Group Candidacy/ZBS-count and scan path selection relationships 158
Figure 9-8 — Example Series Scan Path with a String Path selected in a chip of interest 163
Figure 9-9 — Example of DTS-generated string-write data for three trailing bits 163
Figure 9-10 — String Scan Path characteristics in a Series Scan Topology 164
Figure 9-11 — Conceptual view of the Enumerate Scan Path 164
Figure 9-12 — Enumerate Scan Path characteristics in a Star-4 Scan Topology 170
Figure 9-13 — Conceptual view of command processing 177
Figure 9-14 — Conceptual view of command processor 178
Figure 9-15 — Conceptual view of EPU Scan Paths 179
Figure 10-1 — Conceptual view of the EPU reset logic and state machines 180

Figure 10-2 — Reset State Machine 184
Figure 10-3 — Conceptual view of reset function 185
Figure 10-4 — Test Reset setup time 187
Figure 10-5 — A Type-0 through Type-2 Reset invoking the use of the Standard Protocol 192
Figure 10-6 — A Type-3 Reset invoking the use of the Standard Protocol 193
Figure 10-7 — A Type-4 Reset invoking the use of the Standard Protocol 194
Figure 10-8 — Type-0 through Type-2 Resets invoking Offline-at-Start-up operation 194
Figure 10-9 — A Type-3 Reset invoking Offline-at-Start-up operation 195
Figure 10-10 — Escape Detection 197
Figure 10-11 — Selection Escape followed by a Selection Sequence 198
Figure 10-12 — Conceptual view of the Escape Detection function 199
Figure 10-13 — Selection-Alert Bit Sequence 203
Figure 10-14 — Selection Alert LFSR for bit sequence generation 203
Figure 10-15 — TMSC delay options 204
Figure 10-16 — Selection Alert support logic 205
Figure 10-17 — Deselection Alert operation 207
Figure 10-18 — Selection Alert with embedded Selection Escape 209
Figure 10-19 — Falling-edge ADTAPC State Machine 210
Figure 11-1 — Conceptual view of technology selection mechanism 212
Figure 11-2 — Online/Offline operation with a TAP.7 Controller 213
Figure 11-3 — Online/Offline operation with another technology/RSU with Escapes 215
Figure 11-4 — Online/Offline operation with another technology/RSU with Alerts 215
Figure 11-5 — Offline initiation events 216
Figure 11-6 — Online initiation events 218
Figure 11-7 — TAP.7 Selection Sequence 221
Figure 11-8 — Conceptual view of TAP.7 Controller Selection Sequence 222
Figure 11-9 — Selection Escape/subsequent data timing relationship 226
Figure 11-10 — Selection Alert/subsequent data timing relationship 226
Figure 11-11 — Serial load and initialization of Global Registers 229
Figure 11-12 — CP format 231
Figure 11-13 — TAPC parking-state creation with a deselection Escape/Standard Protocol 233
Figure 11-14 — TAPC parking-state creation with a Selection Escape/Standard Protocol 234
Figure 11-15 — TAPC parking state/Selection Escape/the Advanced Protocol/relationship 234
Figure 11-16 — TAPC parking state/Deselection Escape/the Advanced Protocol/relationship 235
Figure 11-17 — Conceptual view of the Control State Machine 236
Figure 11-18 — CSM *TEST* state function 243
Figure 11-19 — Substates of the CSM *CHK* state 248
Figure 11-20 — A CP_NOP Directive initiated extension of the CP Body Element 248
Figure 11-21 — A CP_END Directive followed by Offline operation 249
Figure 11-22 — A CP_END Directive followed by the use of the Standard Protocol 249
Figure 11-23 — A CP_END Directive followed by the use of the Advanced Protocol 250
Figure 11-24 — A CP_RSO Directive initiating a Type 3 TAP.7 Controller reset 250
Figure 11-25 — CP template 251
Figure 11-26 — *OLS* Selection Escape qualification sequence 254
Figure 11-27 — Simultaneous Selection Escape qualification and TAPC state initialization 255
Figure 11-28 — Conceptual view of the CSM with all sub-states exposed 257
Figure 11-29 — Counter supporting function of the *OLS* state 258
Figure 12-1 — Conceptual view of TAP.7 signal functions 264
Figure 12-2 — Conceptual view of bias for TAP.7 input and input/output signal functions 265
Figure 12-3 — Online-at-Start-up Test Mode Select/signal bias relationships 269
Figure 12-4 — Offline-at-Start-up Test Mode Select/signal bias relationships 270
Figure 12-5 — A Type-0–Type-2 Reset initiating Offline-at-Start-up operation 271
Figure 12-6 — Test Mode Select signal bias changes 274
Figure 12-7 — Test Data Input/signal bias relationships for legacy operation 276
Figure 12-8 — Test Data Output/signal bias relationships 279
Figure 13-1 — TDO(C) Drive Policy/factor relationships 288

Figure 13-2 — Hierarchical view of the TDO(C) Drive Policy 293
Figure 13-3 — Flattened view of the TDO(C) Drive Policy 294
Figure 13-4 — Conceptual view of TDOC Drive Policy 295
Figure 13-5 — T0 TAP.7 TDO Drive Policy 296
Figure 13-6 — T1–T2 TAP.7 TDO Drive Policy 298
Figure 13-7 — T3, T4(W), and T5(W) TAP.7 TDOC Drive Policies 300
Figure 13-8 — Conceptual view of the Scan Group Candidate Count operation 309
Figure 13-9 — *SGCC* and *PSGMCL* timing relationships 312
Figure 13-10 — SSD State/Delayed SSD State/timing relationships 314
Figure 13-11 — Conceptual view of the Conditional Group Membership Count operation 317
Figure 13-12 — Only Conditional Group Member determination 318
Figure 13-13 — Example of TDOC Drive Policy for a T3 and above TAP.7 321
Figure 13-14 — Conceptual view of SGCC and PSGMCL State Machines 323
Figure 13-15 — Determining Scan Group Only Member Last/Membership Count Last 323
Figure 13-16 — Conceptual view of CGMC state development 324
Figure 14-1 — SP content preview 325
Figure 14-2 — SP payload template 326
Figure 14-3 — Transport Packet content preview 327
Figure 14-4 — TMSC Advanced Protocol drive characteristics 328
Figure 14-5 — The TMSC Signal's Distributed Drive Policy 329
Figure 14-6 — Precharge Bit Drive Policy 331
Figure 14-7 — RDY Bit Drive Policy 333
Figure 14-8 — CLTAPC selection state/STL sourced output value relationships 335
Figure 14-9 — Correlation of TDO(C) and TDO Bit Drive Policies 337
Figure 14-10 — TDO Bit Drive Policy 338
Figure 14-11 — Transport Bit Drive Policy 340
Figure 14-12 — Conceptual view of TMSC signal output and miscellaneous support logic 342
Figure 14-13 — Conceptual view of TMSC data and drive enables 343
Figure 15-1 — Inclusion and exclusion of the STL from the scan path 347
Figure 15-2 — Conceptual view of the operation of an EMTAPC 348
Figure 16-1 — Deployment of the T0 TAP.7 350
Figure 16-2 — SoC with IEEE 1149.7 multiple TAPC architecture 351
Figure 16-3 — Operating mode changes/*Run-Test/Idle* state relationships 354
Figure 16-4 — Example IEEE 1149.7 multi-TAP architecture with IR-controlled TAPC exclusion 355
Figure 16-5 — IR Scan Path after the CLTAPC has exited the *Test-Logic-Reset* state and entered the *Run-Test/Idle* state. 356
Figure 16-6 — DR Scan Path with the *IDCODE* instruction loaded in the CLTAPC IR. 356
Figure 16-7 — DR selection with the TAPC_SELECT_NNN instruction loaded in the CLTAPC IR 357
Figure 16-8 — Example IEEE 1149.7 multi-TAP architecture to allow isolating of individual TAPCs under CLTAPC IR control 358
Figure 16-9 — Example IEEE 1149.7 multi-TAP architecture with DR-controlled TAPC exclusion or isolation 360
Figure 16-10 — Example IEEE 1149.7 multi-TAP architecture to allow control over the operating mode of individual TAPCs by using *tapc_select* chip signals 361
Figure 16-11 — Conceptual view of the TAP_QUERY instruction 362
Figure 16-12 — Example system 363
Figure 16-13 — Example of the active *BYPASS* instruction 368
Figure 16-14 — Package-level connectivity of the POR* and nTRST signals 370
Figure 16-15 — The DR-wire solution in the SiP-TAP approach 371
Figure 17-1 — Conceptual view of zero bit DR Scan detection 375
Figure 17-2 — Conceptual view of ZBS count locking 376
Figure 17-3 — TAPC-state/control-state and ZBS-count relationships 378
Figure 17-4 — EPU Operating States 378
Figure 17-5 — ZBS use state and ZBS-count control flow 381
Figure 17-6 — Conceptual view of the ZBS use states with both TAP.7 and other ZBS use 383
Figure 18-1 — Conceptual view of a T1 TAP.7 386

Figure 18-2 — Deployment of the T1 TAP.7 ... 387
Figure 18-3 — Conceptual view of *nsys_trst* and *sys_tms* generation ... 394
Figure 18-4 — Conceptual view of functional reset request generation ... 397
Figure 18-5 — Conceptual view of function reset request timing/system-initiated clear ... 397
Figure 18-6 — Conceptual view of function reset request timing with DTS-initiated clear ... 398
Figure 18-7 — Components involved in TAP.7 Controller power management ... 402
Figure 18-8 — TAP.7 Controller power-management state progression ... 404
Figure 18-9 — TAP.7 power-manager operation ... 406
Figure 18-10 — Conceptual view of the TAP.7 power manager ... 407
Figure 18-11 — Typical power-mode interface ... 408
Figure 18-12 — Directed power-up of a TAP.7 Controller ... 409
Figure 18-13 — Detected power-up of a TAP.7 Controller ... 410
Figure 18-14 — Conceptual operation of TAP.7 Controller power control ... 411
Figure 18-15 — TAP.7 Controller power-management responsibilities ... 411
Figure 18-16 — Power-down criteria selection ... 412
Figure 18-17 — Mode 2 – TAP.7 Controller and STL shutdown ... 414
Figure 18-18 — Mode 0 – with a TCK TIMEOUT initiating power-down ... 415
Figure 18-19 — Mode 1 – with the *Test-Logic-Reset* state and TCK TIMEOUT initiating power-down ... 415
Figure 18-20 — Mode 2—with the *Test-Logic-Reset* state initiating power-down ... 415
Figure 18-21 — Power-down logic example ... 416
Figure 18-22 — Power-down request generation flowchart ... 418
Figure 18-23 — Power-down criteria selection ... 419
Figure 18-24 — Default Power-Control Mode ... 419
Figure 18-25 — A PD_STOP initiating a Type-3 TAP.7 Controller reset ... 421
Figure 19-1 — Typical T2 TAP.7 ... 424
Figure 19-2 — Deployment of the T2 TAP.7 ... 425
Figure 19-3 — *Run-Test/Idle*/Control Path/Scan Group Candidacy relationships ... 431
Figure 19-4 — Skewed *Run-Test/Idle*/Control Path/Scan Group Candidacy relationships ... 432
Figure 19-5 — TAP.7 Controller reset creating *Test-Logic-Reset* parking state ... 433
Figure 19-6 — Re-synchronization of ADTAPC and CLTAPC states following assertion of *nsys_trst* ... 434
Figure 19-7 — Conceptual view of T2 TAP.7 Scan Group Membership management ... 435
Figure 19-8 — Conceptual view of T2 TAP.7 current Scan Group Candidacy development ... 435
Figure 19-9 — CLTAPC selection state change/*Run-Test-Idle_f*/register relationships ... 437
Figure 19-10 — CLTAPC selection state change/*Test-Logic-Reset_f* ... 437
Figure 20-1 — T3 TAP.7 ... 441
Figure 20-2 — Deployment of the T3 TAP.7 ... 442
Figure 20-3 — TDOC output with the JScan3 Scan Format within the CR Scan ... 452
Figure 20-4 — CID allocation with a DTS-sourced AT ... 453
Figure 20-5 — CID allocation with a TS-sourced AT ... 453
Figure 20-6 — Conceptual view of CID and CIDI Registers ... 454
Figure 20-7 — Conceptual view of an SSD ... 458
Figure 20-8 — SSDs detection and completion regions ... 460
Figure 20-9 — Conceptual view of SSD Processing State Machine ... 461
Figure 20-10 — SSD Interlocking State Machine ... 463
Figure 20-11 — SSD detection and completion window ... 466
Figure 20-12 — SSDs changing the Scan Group Membership in the *RTI* state ... 467
Figure 20-13 — SSD_SA ignored because of early exit from the *RTI* state ... 468
Figure 20-14 — SSDs changing the Pause Selection state ... 469
Figure 20-15 — SSD_SA ignored in the *Pause-xR* state ... 470
Figure 20-16 — Conceptual view of SSD processing ... 471
Figure 20-17 — Conceptual view of SSD state and SSD state delayed ... 471
Figure 20-18 — Conceptual view of TCA and CID comparison ... 472
Figure 20-19 — TMS and reset value required for SSD to perform its designated function ... 474
Figure 20-20 — SSD effects ... 476
Figure 20-21 — Scan topology characteristics used in Scan Topology Training ... 479

Figure 20-22 — Conceptual view of current Scan Group Candidacy development—T3 and above TAP.7s 482
Figure 20-23 — Current Scan Group Candidacy development T3 and above TAP.7s 482
Figure 20-24 — Group membership operation 484
Figure 20-25 — Saved Scan Group Candidacy operation 485
Figure 20-26 — *sys_tck* gating/Scan Group Membership change relationships 485
Figure 21-1 — T4 and above TAP.7 chip block diagram 487
Figure 21-2 — Conceptual view of fully deployed APU functionality 488
Figure 21-3 — Conceptual block diagram of the APU and RSU functions 491
Figure 21-4 — APU/EPU interface 496
Figure 21-5 — APU/DCC(s) interface 497
Figure 21-6 — Conceptual view of TAP.7 use with a T5 TAP.7 Controller 498
Figure 21-7 — APU functions/APU Operating State relationships 499
Figure 21-8 — Operating state sequence examples 501
Figure 21-9 — Typical DTS-initiated packet sequences and APU state transitions 503
Figure 21-10 — Packet combinations used to advance the TAPC state 505
Figure 21-11 — Conceptual view of packet scheduling 508
Figure 21-12 — Example of scheduling and sequencing of state machine activity 510
Figure 21-13 — Advanced operation function/description relationships 511
Figure 22-1 — Conceptual view of a Scan Packet 513
Figure 22-2 — Scan exchange types 516
Figure 22-3 — Voting bit transaction 517
Figure 22-4 — Master/Slave bit transaction 517
Figure 22-5 — Scripted scan exchange 517
Figure 22-6 — Conceptual view of a TP 519
Figure 22-7 — TP placement and content 520
Figure 22-8 — APU state diagram 521
Figure 22-9 — Use of the virtual TAPC state 522
Figure 22-10 — Conceptual view of a Scan Packet Element scheduling 523
Figure 23-1 — Deployment of the T4 TAP.7 525
Figure 23-2 — Advanced Scan Format overview 533
Figure 23-3 — TAP.7 data path with positive- and negative-edge clocking 538
Figure 23-4 — The *sys_tck* signal 538
Figure 23-5 — Example of the MScan Scan Format with *sys_tck* signal duty-cycle options 539
Figure 23-6 — *sys_tck* signal logic 1 time 539
Figure 23-7 — Conceptual view of APFC operation 540
Figure 23-8 — SREDGE/tmsc_mux/tmsc_r relationships 541
Figure 23-9 — Conceptual view of *sys_tms* generation for a T4 and above TAP.7 542
Figure 23-10 — Conceptual view of TMS generation with the Advanced Protocol 543
Figure 23-11 — Conceptual view of *sys_tdi* signal generation for a T4 and above TAP.7 544
Figure 23-12 — Conceptual view of System Ready treatment in its simplest form 546
Figure 23-13 — Conceptual *sys_rdy* generation for more complex use cases 547
Figure 23-14 — Conceptual view of TDO data generation for output via the TMSC signal 548
Figure 23-15 — Using the TMSC value in next state equations 551
Figure 24-1 — Application types supported by the MScan Scan Format 553
Figure 24-2 — High-level operation of the MScan Scan Format 553
Figure 24-3 — Scan Packet Elements with the MScan Scan Format 554
Figure 24-4 — MScan payload template 555
Figure 24-5 — MScan payload/EPU input and output relationships 556
Figure 24-6 — MScan output bit-frame 556
Figure 24-7 — MScan output bit-frame with stalled completion 557
Figure 24-8 — Typical TCKC and TMSC signal system delays 557
Figure 24-9 — Use of [RDY] bit(s) to accommodate propagation delays 558
Figure 24-10 — Delay Element format 559
Figure 24-11 — MScan SPs with Delay Elements 560
Figure 24-12 — Type-3 Reset generated by a variable-length Delay Element 561

Figure 24-13 — MScan SP payload/TAPC state advance relationship 562
Figure 24-14 — CID allocation with MScan SPs 563
Figure 24-15 — Conceptual view of MScan SP Payload Element behavior 565
Figure 24-16 — Conceptual view of the Payload State Machine for the MScan Scan Format 566
Figure 24-17 — Conceptual view of Ready State Machine MScan operation 567
Figure 24-18 — Conceptual Delay Element operation 567
Figure 24-19 — Conceptual view of the Delay State Machine 568
Figure 25-1 — Application types supported by OScan Scan Formats 570
Figure 25-2 — High-level operation of the OScan Scan Formats 571
Figure 25-3 — Scan Packet Elements with the OScan Scan Format 571
Figure 25-4 — OScan payload template 572
Figure 25-5 — Payloads for *Shift-xR* and non-*Shift-xR* TAPC states 573
Figure 25-6 — EPU input/output relationships with an nTDI, TMS, RDY, and TDO SP payload 575
Figure 25-7 — EPU input/output relationships with a TMS SP payload 575
Figure 25-8 — EPU input/output relationships with an nTDI, RDY, and TDO SP payload 576
Figure 25-9 — EPU input/output relationships with an nTDI SP payload 576
Figure 25-10 — EPU input/output relationships with an nTDI/TDO SP payload 577
Figure 25-11 — TMS generation with an EOT Escape 577
Figure 25-12 — OScan6 PAD bit and its function 578
Figure 25-13 — OScan output bit-frame 579
Figure 25-14 — OScan/SScan bit-frame with stalled completion 579
Figure 25-15 — Using delays with the OScan Scan Formats 581
Figure 25-16 — OScan6 SP payload/TAPC state advance relationship 583
Figure 25-17 — Virtual TAPC state with OScan6 Scan Format 583
Figure 25-18 — Example with the *sys_tck* signal duty-cycle options with OScan1 585
Figure 25-19 — Conceptual view of OScan SP Payload Element behavior 586
Figure 25-20 — Conceptual view of Payload State Machine entry point generation 587
Figure 25-21 — Shift Progress flag for OScan6 support 588
Figure 25-22 — CSM and SSM activation 588
Figure 25-23 — Conceptual view of Ready State Machine OScan/SScan operation 589
Figure 25-24 — Conceptual view of TAP advance with MScan/OScan Scan Formats 589
Figure 26-1 — Application types supported by SScan Scan Formats 591
Figure 26-2 — Stall profile/application relationships 594
Figure 26-3 — SScan segment use cases 595
Figure 26-4 — SScan transactions with a TAP.1-like component 596
Figure 26-5 — SScan transactions with a DMA or FIFO 596
Figure 26-6 — SScan transactions with an FIFO 597
Figure 26-7 — SScan transactions with rate-dependent components 597
Figure 26-8 — SScan transactions with a buffered rate-dependent component 598
Figure 26-9 — Stall profile combinations 598
Figure 26-10 — Scan Packet Elements with the SScan Scan Formats 600
Figure 26-11 — Header Element of an SP 601
Figure 26-12 — SP payloads for *Shift-xR* and non-*Shift-xR* TAPC states 603
Figure 26-13 — Segment composition 607
Figure 26-14 — SScan input-only and input/output Data Segment processing 608
Figure 26-15 — SScan0/SScan1 output-only Data Segment processing 611
Figure 26-16 — SScan2/3 output-only Data Segment processing 612
Figure 26-17 — TDO pipelining with the SScan2/SScan3 Scan Formats 613
Figure 26-18 — CLTAP TDO pipelining with SScan2/SScan3 Scan Formats/with stalls 614
Figure 26-19 — Using delays with the SScan Scan Formats 618
Figure 26-20 — Packets following an SP associated with the *Update-DR* and other states 619
Figure 26-21 — Packets following an SP associated with the *Capture-xR/Exit2-xR states* 620
Figure 26-22 — SScan0/1 TAPC state advance examples 623
Figure 26-23 — SScan2/3 TAPC state advance examples for I/O and input-only segments 624
Figure 26-24 — SScan2/3 TAPC state advance examples for output-only segments 625
Figure 26-25 — Conceptual view of the Payload State Machine with Header handling 627

Figure 26-26 — Conceptual view of the Escape Detection State Machine 629
Figure 26-27 — SScan Shift Progress flag 630
Figure 26-28 — Conceptual view of TAP advance with MScan/OScan/SScan Scan Formats 630
Figure 26-29 — SScan entry point reload additions for output only 631
Figure 26-30 — Conceptual view of Header Register 631
Figure 26-31 — Conceptual view of Payload State Machine entry point with SScan support 632
Figure 26-32 — Joint operation of the state machines 633
Figure 26-33 — Joint operation of state machines with Command Part Two *Update-DR* 633
Figure 27-1 — Conceptual view of T5 TAP.7 Transport Function 635
Figure 27-2 — Deployment of a T5 TAP.7 Controller 636
Figure 27-3 — Conceptual view of T5 TAP.7 Controller configurations 644
Figure 27-4 — TP placement and content 648
Figure 27-5 — Transport Packet Elements 649
Figure 27-6 — TP Directive Elements and their surrounding context 651
Figure 27-7 — Directive/transport building block relationships 652
Figure 27-8 — Summary of Register Element characteristics 660
Figure 27-9 — Summary of Data Element characteristics 663
Figure 27-10 — Selection mechanisms for data and register transfers 665
Figure 27-11 — Operation of the DCCy_ENAR and DCCy_ENAA register bits 665
Figure 27-12 — Operation of the DCCy_DCNR and DCCy_DRNA register bits 666
Figure 27-13 — Conceptual view of T5 TAP.7 transport control 668
Figure 27-14 — Conceptual view of transport control facilitating a data exchange 669
Figure 28-1 — *TPA* state behaviors 673
Figure 28-2 — *TPA* state flow 674
Figure 28-3 — TP Directive Element format, timing, and TMSC signal drive characteristics 675
Figure 28-4 — A Type-3 Reset generated by the TP_RSZ and TP_RSO Directives 675
Figure 28-5 — TP Register Element format, timing, and TMSC signal drive characteristics 676
Figure 28-6 — Register Element with surrounding TP Directives 677
Figure 28-7 — TP Data Element format, timing, and TMSC signal drive characteristics 680
Figure 28-8 — Fixed-length Data Payload with surrounding TP Directives 680
Figure 28-9 — Variable-length Data Payload with surrounding headers 681
Figure 28-10 — DCCy_DIRA Register/Data Payload content relationships 682
Figure 28-11 — Data payload and data channel data alignment relationship 683
Figure 28-12 — Conceptual view of the Transport State Machine 685
Figure 28-13 — Queuing a TP to follow an SP 687
Figure 28-14 — Queuing a TP to follow an SP with the OScan2 Scan Format 688
Figure 28-15 — Queuing a TP to follow an SP with the OScan1 Scan Format 689
Figure 28-16 — Starting directive processing/ending TP processing 690
Figure 28-17 — PDCx/DCC interface signals with a single DCC connected to the DCC 691
Figure 28-18 — PDCx/DCC interface signals with multiple DCCs sharing the PDC 692
Figure 28-19 — Conceptual view of T5 TAP.7 Transport Control 695
Figure 28-20 — PDCx/DCC interface signaling/TP_NOP and TP_END Directives 699
Figure 28-21 — DCC interface signaling/TP_DCx Directives 700
Figure 28-22 — PDCx/DCC interface signaling/nonterminating eight-bit directives 701
Figure 28-23 — PDCx/DCC interface signaling/TP_RSO and TP_RSZ Directives 702
Figure 28-24 — PDCx/DCC interface signaling/12-bit directives other than TP_CRR/TP_CRW 703
Figure 28-25 — PDCx/DCC interface signaling with the TP_CRR Directive 704
Figure 28-26 — PDCx/DCC interface signaling with the TP_CRW Directive 705
Figure 28-27 — DCC interface signaling required for Custom Operation 706
Figure 28-28 — Pipelining data transfers 706
Figure 28-29 — Conceptual view of the Transport Function 707
Figure 28-30 — Example Transport State Machine 708
Figure 28-31 — Behavior of the *next_dir* signal 709
Figure 28-32 — Multi-use Register bit input configurations 710
Figure 28-33 — Multi-use Register values/TSM relationships 712
Figure 28-34 — Transport drive and DCR input selection 716

Figure 28-35 — TP with fixed-length data transfer with nonpipelined scan operations 718
Figure 28-36 — TP with fixed-length data transfer with pipelined scan operations 719
Figure 28-37 — TP with continuous data transfer 720
Figure 28-38 — TP with no data transferred 721
Figure 29-1 — Typical test application – testing component interconnections 724
Figure 29-2 — Unit-under-test description 729
Figure 31-1 — Serial connection using one TMS signal 767
Figure 31-2 — Connection in two paralleled serial chains 769
Figure 31-3 — Basic Star Scan Topology 770
Figure 31-4 — Basic hierarchical topology 771
Figure A-1 — IEEE 1149.1 TAPC State Machine 775
Figure A-2 — IEEE 1149.1 signaling 776
Figure A-3 — Zero-bit DR Scan state sequences, path A 776
Figure A-4 — Zero-bit DR Scan state sequences, path B 777
Figure B-1 — MScan and OScan SP content 778
Figure B-2 — MScan transaction 780
Figure B-3 — OScan0 transaction 781
Figure B-4 — OScan1 transaction 782
Figure B-5 — OScan2 transaction 783
Figure B-6 — OScan3 transaction 784
Figure B-7 — Oscan4 transaction 785
Figure B-8 — OScan5 transaction 786
Figure B-9 — OScan6 transaction 788
Figure B-10 — OScan7 transaction 789
Figure B-11 — SScan0 transaction/first SP stall profile 792
Figure B-12 — SScan0 transaction/all stall profile 793
Figure B-13 — SScan1 transaction/first SP stall profile 795
Figure B-14 — SScan1 transaction/no stall profile 796
Figure B-15 — SScan2 transaction/first SP stall profile 798
Figure B-16 — SScan2 transaction/all stall profile 799
Figure B-17 — SScan3 transaction/first stall profile 801
Figure B-18 — SScan3 transaction/no stall profile 802
Figure B-19 — OScan1 Scan Format/TPs with fixed-length Data Element following SPs 803
Figure B-20 — OScan7 Scan Format/TPs with fixed-length Data Element following SPs 803
Figure B-21 — OScan1 Scan Format/TPs with variable-length Data Element following SPs 804
Figure B-22 — OScan7 Scan Format/TPs with variable-length Data Element following SPs 804
Figure D-1 — Power-control states 849
Figure D-2 — Consolidated view of CSM states 850
Figure D-3 — TAP initialization and topology determination 852
Figure D-4 — TS initialization 854
Figure D-5 — Scan Topology Training 859
Figure D-6 — Branch interrogation 860
Figure D-7 — Series Branch interrogation 863
Figure D-8 — Reads of CNFG0–CNFG3 Registers in a Series Scan Topology 864
Figure D-9 — Determining the type/class of series TAPs 866
Figure D-10 — Star-4 Branch interrogation—part one 868
Figure D-11 — Star-4 Branch interrogation—part two 869
Figure D-12 — Star-2 Branch interrogation—part one 871
Figure D-13 — Star-2 Branch interrogation—part two 872
Figure E-1 — Electrical characteristics 876
Figure F-1 — Typical TCK(C) frequency versus number of TAPs 879
Figure F-2 — Connection topologies 880
Figure F-3 — Series termination scheme 881
Figure F-4 — Parallel termination schemes 881
Figure F-5 — The use of input buffers with hysteresis 882
Figure F-6 — Signal filtering using a one shot 882

Figure F-7 — Model of circuit used to compare the rise/fall time effects on signal quality 884
Figure F-8 — Overshoot and undershoot with the output driver's rise/fall time at 0.5 ns 884
Figure F-9 — Overshoot and undershoot with the output driver's rise/fall time at 1.5 ns 885
Figure F-10 — Lumped load 886
Figure F-11 — Distributed load 886
Figure F-12 — Series termination with impedance mismatch causing under/overshoots 889
Figure F-13 — Series termination with impedance mismatch causing monotonicity issues 890
Figure F-14 — Proper connection of TAP signaling on a board a Line configuration 892
Figure F-15 — Proper connection of TAP signaling on a board and T configuration 892
Figure F-16 — Proper connection of TAP signaling on a board and X configuration 892
Figure F-17 — Improper connection of TAP signaling on a board with parallel termination 893
Figure F-18 — Proper connection of TAP signaling with more than one connection 893
Figure F-19 — Basic series termination waveform 894
Figure F-20 — Simple parallel DC termination 895
Figure F-21 — Ideal parallel DC termination 896
Figure F-22 — Parallel DC termination, 2 ns edge-rates, four 3 picofarad loads 897
Figure F-23 — Realistic parallel termination model 897
Figure F-24 — Realistic AC parallel termination model 898
Figure F-25 — Ideal parallel AC termination, No Load 899
Figure F-26 — Parallel AC termination model with one load 899
Figure F-27 — Parallel AC termination simulation results 900
Figure F-28 — Basic parallel termination waveform with capacitive load isolation 902
Figure F-29 — DTS and chip models 903
Figure F-30 — Programmable DTS source impedance 903
Figure F-31 — DTS input capacitance load isolation 904
Figure F-32 — Emitter-follower driver 905
Figure F-33 — Voltage translator 906
Figure F-34 — Point-to-Point transmission-line model 908
Figure F-35 — Point-to-Point/series termination 908
Figure F-36 — One source/one destination/unidirectional signaling/parallel AC termination 909
Figure F-37 — Single source/destination/bidirectional signaling/series termination 909
Figure F-38 — Bidirectional scenario—DTS drives/chip/TAPC receives 910
Figure F-39 — Bidirectional scenario—Chip/TAPC drives, DTS receives 910
Figure F-40 — Line configuration of a transmission line with series termination 911
Figure F-41 — Model for a line transmission line with 1 to 16 TAPs 912
Figure F-42 — Line configuration, two loads—25 mm intervals, 50 mm DTC trace 914
Figure F-43 — Line configuration, four loads—25 mm intervals, 50 mm DTC trace 915
Figure F-44 — Line configuration, eight loads—25 mm intervals, 50 mm DTC trace 916
Figure F-45 — Line configuration, 16 loads—25 mm intervals, 50 mm DTC trace 917
Figure F-46 — Multiple TAP connection to a Line configuration 918
Figure F-47 — Parallel AC termination, one load at end of transmission line 919
Figure F-48 — Parallel AC termination, four loads at 25 mm intervals 919
Figure F-49 — Bidirectional scenario—chip/TAPC drives, DTS receives, multiple TAPCs 921
Figure F-50 — Bidirectional multiple TAPCs, 100 MHz, R_{ISO} = 10 Ω 922
Figure F-51 — Bidirectional multiple TAPCs, 100 MHz, R_{ISO} = 50 Ω 922
Figure F-52 — Line configuration, bidirectional multiple TAPCs, 40 MHz, R_{ISO} = 50 Ω 923
Figure F-53 — Line configuration, 4 TAPs, C2 and C3 drive, 50 MHz 924
Figure F-54 — Line configuration 4 TAPs, C2 and C4 drive, 50 MHz 925
Figure F-55 — Line configuration, four TAPs, four drive, 50 MHz 926
Figure F-56 — Line configuration: 8 TAPs, two drive (C1 and C6 drive), 50 MHz 927
Figure F-57 — Line configuration: 8 TAPs, two drive (C2 and C4), 50 MHz 928
Figure F-58 — Line configuration: 8 TAPs, two drive (C2 and C6), 50 MHz 929
Figure F-59 — Logical view of T configuration of a transmission line 930
Figure F-60 — T model with parallel DTS drivers and two nodes/leg 931
Figure F-61 — Impedance profile of the T configuration 932
Figure F-62 — T configuration: 4 TAPs, DTS drive, 50 MHz 933

Figure F-63 — T configuration, 4 TAPs, U1A drives, 50 MHz 934
Figure F-64 — T configuration, 4 TAPs, one drive (U1B), 50 MHz 935
Figure F-65 — T configuration, 4 TAPs, two drive (U1A and U1B), 50 MHz 936
Figure F-66 — T configuration, 4 TAPs, two drive (U1B and U1D drive), 50 MHz 937
Figure F-67 — Logical view of X configuration of a transmission line 938
Figure F-68 — X model with parallel DTS drivers and four nodes/leg 939
Figure F-69 — Contrasting matched and unmatched source and load impedances 940
Figure F-70 — X configuration, 8 TAPs, DTS drive, 100 MHz, at destination 940
Figure F-71 — X configuration. 8 TAPs, DTS drive, 50 MHz 941
Figure F-72 — X configuration, 8 TAPs, two TAPs/leg, one drive (U1A), 50 MHz 942
Figure F-73 — X configuration, 8 TAPs, two TAPs/leg, one drive (U1B), 50 MHz 943
Figure F-74 — X configuration, 8 TAPs, two TAPs/leg, two drive (U1A and U1B), 50 MHz 944
Figure F-75 — X configuration, 8 TAPs, two TAPs/leg, four drive, 50 MHz 945
Figure F-76 — X configuration, 8 TAPs, two TAPs/leg, all drive, 50 MHz 946
Figure F-77 — Logical view of XT configuration of a transmission line 947
Figure F-78 — Impedance profile of the XT configuration 947
Figure F-79 — Bidirectional, balanced delay, 16 TAPCs, detailed model 948
Figure F-80 — XT configuration, 16 TAPs, nodes driven by DTS, 50 MHz, at destination 949
Figure F-81 — XT configuration, DTS drive, 50 MHz, at source 950
Figure F-82 — XT configuration, 16 TAPs, one drives (U1A), 50 MHz 951
Figure F-83 — XT configuration, 16 TAPs, one drives (U1B), 50 MHz 952
Figure F-84 — XT configuration, 16 TAPs, one drive and neighbor, 50 MHz 953
Figure F-85 — XT configuration, 16 TAPs, two drive, 50 MHz 954
Figure F-86 — XT configuration, 16 TAPs, four drive, 50 MHz 955
Figure F-87 — XT configuration, 16 TAPs, all drive, DTS observed, 50 MHz 956
Figure F-88 — Recommended series termination scheme with one to four chips 958
Figure F-89 — Recommended parallel termination scheme with one to four chips 958
Figure F-90 — Recommended series termination scheme for highest performance four/six chips 959
Figure F-91 — Determining signal load classification 959
Figure G-1 — SScan0/SScan2 DMA Transfers 962
Figure G-2 — SScan0/SScan2 transfers with Paced Block 964
Figure G-3 — Example RDY generation for SScan1 or SScan3 Paced-Block transfers 965
Figure G-4 — SScan1/SScan3 mixed Paced-Bit and Paced-Block transfers 965
Figure H-1 — An IEEE 1149.1 TAP with RTCK signal 967
Figure H-2 — Expected behavior for the RTCK and TCK 967
Figure H-3 — Unexpected behavior for RTCK 968
Figure H-4 — RTCK connected to an APU 968
Figure H-5 — RTCK generation for multiple TAPs 969
Figure H-6 — System-wide RTCK behavior 970
Figure H-7 — System-wide RTCK generation logic 970
Figure H-8 — Exclusion of TAP which outputs RTCK2 971
Figure H-9 — Inclusion of TAP which outputs RTCK2 971
Figure H-10 — RTCK behavior after a TAP.7 Controller power-up 972
Figure H-11 — RTCK behavior with Standard-to-Advanced Protocol change 972
Figure H-12 — RTCK behavior with Advanced-to-Standard Protocol change 973
Figure H-13 — Use of the RTCK signal as an auxiliary function 973

Tables

Table 1-1 — TAP.7 signal list 12
Table 1-2 — TAP.7 Class and scan topology relationships 13
Table 1-3 — Relationship TAPC state name alias/TAPC state 23
Table 1-4 — Table Format 24
Table 4-1 — TAPC hierarchy/allowed TAPC parking-state relationships 41
Table 4-2 — Selection state terminology summary 43
Table 4-3 — Contrast of series and star operation 46
Table 4-4 — TAP.7 Class/Escape relationships 52
Table 4-5 — TAP.7 Class/Protocol relationships 53
Table 6-1 — Events causing TMSC pin utilization changes with a T4 TAP.7 105
Table 6-2 — Events causing TMSC pin utilization changes (with transport) 118
Table 6-3 — TAP.7 feature group summary 121
Table 7-1 — IEEE 1149.1 and IEEE 1149.7 attributes affecting system architectures 122
Table 7-2 — Branch/technology deployment permissibility 124
Table 8-1 — TAP.7 Class relationship to selection capability 130
Table 8-2 — TAPC parent/child relationships 130
Table 8-3 — Selection and deselection states 132
Table 9-1 — TAP.7 Controller register list managed commands 145
Table 9-2 — Reset values of TAP.7 Controller registers managed with commands 146
Table 9-3 — TAP.7 Controller command list 147
Table 9-4 — TAP.7 Controller command definition 151
Table 9-5 — Command, TAPC State Machine states, and ZBS representations in examples 154
Table 9-6 — TAP.7 Scan Path for IR Scans 157
Table 9-7 — TAP.7 Scan Path data for DR Scans 158
Table 9-8 — EPU Scan Path selection/control level relationships 160
Table 9-9 — EPU Scan Path utilization with control level two 160
Table 9-10 — Factors causing selection of the bit, string, and auxiliary paths 160
Table 9-11 — Scan counts for string operations in a Series Scan Topology 163
Table 9-12 — EPU Scan Path characteristics 165
Table 9-13 — RDBACK0 Register format 172
Table 9-14 — RDBACK1 Register format 172
Table 9-15 — Configuration Register zero format 175
Table 9-16 — Configuration Register one format 176
Table 9-17 — Configuration Register two and three format 176
Table 10-1 — Reset effects 182
Table 10-2 — Reset state descriptions 184
Table 10-3 — Conditions causing assertion of reset types 185
Table 10-4 — Reset effects and references 186
Table 10-5 — Start-up option determination 191
Table 10-6 — TAP.7 Class/Start-up option relationships 191
Table 10-7 — Reset values for TAP.7 Start-up options 192
Table 10-8 — TAP.7 Class/Escape deployment relationships 196
Table 10-9 — Escapes 201
Table 10-10 — Selection Alert sequence 206
Table 11-1 — Online Activation Code 225
Table 11-2 — Extension Code 228
Table 11-3 — Drive conflict protection is activated 228
Table 11-4 — Global Register State loaded 230
Table 11-5 — Creation of a TAP.7 Controller TAPC parking state with the Standard Protocol 234
Table 11-6 — Creation of a TAP.7 Controller TAPC parking state with the Advanced Protocol 235
Table 11-7 — TAP.7 Controller behavior in the CSM *STD* state 238

Table 11-8 — TAP.7 Controller behavior while in the CSM *ADV* state 239
Table 11-9 — TAP.7 Controller behavior in the CSM *OLW* state 240
Table 11-10 — TAP.7 Controller behavior while in the CSM *TEST* state 246
Table 11-11 — SCNFMT Register value resulting from the Short-Form Selection Sequence 247
Table 11-12 — OAC value/TOPOL Register relationships required for placement Online 247
Table 11-13 — CP Directives 252
Table 11-14 — TAP.7 Controller behavior while in the CSM *CHK* state 252
Table 11-15 — TAP.7 Controller behavior while in the CSM *OLS* state 256
Table 12-1 — Relationship of TAP.7 Classes/signal names 263
Table 12-2 — Relationship of TAP.7 Classes/Signal Characteristics 264
Table 12-3 — Signal bias effects transferred to signals sharing a connection 266
Table 12-4 — TCK/TCKC signal behavior relationships 267
Table 12-5 — TMS/TMSC signal behavior relationships with start-up Online 275
Table 12-6 — TMS/TMSC signal behavior relationships with start-up Offline 275
Table 12-7 — TDI/TDIC signal behavior relationships 277
Table 12-8 — TDO/TDOC signal behavior relationships 279
Table 12-9 — CLTAPC State Machine walk to provide IEEE 1149.7-Other Behavior 285
Table 13-1 — TAP.7 Class/TDO(C) Drive Policy component applicability 290
Table 13-2 — Defaults for unimplemented functions when determining TDOC Drive Policy 296
Table 13-3 — SGCC state definition 308
Table 13-4 — PSGMCL state definition 309
Table 13-5 — Scan Group Candidate Count operation 311
Table 13-6 — Potential Scan Group Membership Count Last operation 312
Table 13-7 — SGMCL state definition 313
Table 13-8 — Scan Group Membership Count Last operation 313
Table 13-9 — Conditions governing Idle Group Candidacy 315
Table 13-10 — Idle Group Membership 315
Table 13-11 — Conditions governing Pause-IR and Pause-DR Group Membership 315
Table 13-12 — Only Scan Group Member delayed determination 315
Table 13-13 — Conditional Group Member Count state definition 317
Table 13-14 — Operation of the Conditional Group Membership Count State Machine 319
Table 13-15 — Only Conditional Group Member determination 320
Table 13-16 — Signal descriptions in Figure 13-13 322
Table 13-17 — SGCC and PSGMCL State Machine encoding 322
Table 13-18 — CGMC state encoding 324
Table 14-1 — RDY Bit Drive Policies 334
Table 14-2 — TDO Bit Drive Policy with the System Path 338
Table 14-3 — Voting and single enables 339
Table 14-4 — TDO Bit Drive Policy with the Control Paths 339
Table 14-5 — Miscellaneous signal name definitions 341
Table 14-6 — TDO bit data source selection terms 344
Table 15-1 — EMTAPC operation 348
Table 16-1 — Permitted methods to control the EMTAPCs' operating modes 353
Table 16-2 — Permitted combinations of methods for controlling EMTAPCs 353
Table 16-3 — Nomenclature used in description 363
Table 16-4 — An example instruction set for the IR managed by an SiP-TAP 369
Table 17-1 — ZBS detect state definitions 375
Table 17-2 — ZBS count locking states 376
Table 17-3 — ZBS use state characteristics with EPU Operating States 379
Table 17-4 — State description for Figure 17-6 382
Table 17-5 — Control levels 385
Table 18-1 — T1 TAP.7 function/register/command relationships 389
Table 18-2 — T1 TAP.7 Controller register descriptions 391
Table 18-3 — Specifying the use of T1 TAP.7 optional functions 393
Table 18-4 — Precedence of operations affecting the FRESET Register 399
Table 18-5 — TAP.7 Controller power-control mode use cases 400

Table 18-6 — TAP.7 Controller Power-Control Mode use cases 401
Table 18-7 — DTS characteristics required to orchestrate TAP.7 Controller power-down 401
Table 18-8 — Power-down request generation summary 413
Table 18-9 — Power-control states 417
Table 18-10 — Changes to power-down and power-up enables 417
Table 19-1 — T2 TAP.7 function/new register/command relationships 426
Table 19-2 — T2 TAP.7 new register descriptions 427
Table 19-3 — Specifying the use of T2 TAP.7 configurations 428
Table 19-4 — T2 TAP.7 Scan Format characteristics 429
Table 19-5 — Current Scan Group Candidacy creation 434
Table 19-6 — Maximum synchronization stays in *Run-Test/Idle* state 436
Table 19-7 — Factors determining the Scan Selection State for a T2 TAP.7 438
Table 20-1 — T3 TAP.7 function/new register/command relationships 444
Table 20-2 — T3 TAP.7 new register definitions 445
Table 20-3 — T3 TAP.7 Scan Format characteristics 447
Table 20-4 — TCA format 448
Table 20-5 — AT format 451
Table 20-6 — CID allocation support with a T3 TAP.7 455
Table 20-7 — Participation of a TAP.7 Controller in CID allocation 455
Table 20-8 — External-AT derivation during CR Scan *Shift-DR* states 455
Table 20-9 — TDOC behavior/undirected allocation method and JScan3 Scan Format 457
Table 20-10 — Executed SSD/*Run-Test/Idle*/group membership relationships 459
Table 20-11 — Executed SSD/*Pause-xR*/group membership relationships 459
Table 20-12 — SSD Processing State Machine state names 462
Table 20-13 — SSD state description 464
Table 20-14 — SSDs and address payloads 472
Table 20-15 — SSD/SSD state relationships 475
Table 20-16 — Permitted SSD processing 475
Table 20-17 — Scan Selection Directive/SGC relationships 475
Table 20-18 — Scan topology connectivity and continuity tests 479
Table 20-19 — Topology Tests/TOPOL Register relationships 481
Table 20-20 — TOPOL Register initialization 481
Table 21-1 — Transport Function capability 494
Table 21-2 — TAP signal behavior 496
Table 21-3 — Summary of APU Operating State change relationships 500
Table 21-4 — Description of APU Operating State change relationships 502
Table 21-5 — Description of packet combinations 504
Table 21-6 — Packet and TAPC state relationships 507
Table 22-1 — Variable-length delay examples 516
Table 23-1 — T4 TAP.7 function/register/command relationships 526
Table 23-2 — T4 TAP.7 register descriptions 529
Table 23-3 — Specifying the use of T4 TAP.7 optional functions 531
Table 23-4 — STCKDC register relationship to *sys_tck* signal generation 540
Table 23-5 — TMS value when the Advanced Protocol is used 543
Table 23-6 — *sys_tms* signal generation 544
Table 23-7 — TDI value when the Advanced Protocol is used 545
Table 23-8 — *sys_tdi*/*epu_tdi* signal generation 545
Table 23-9 — *epu_tdo_in* signal generation 545
Table 23-10 — SSD detection with a T4 and above TAP.7 550
Table 24-1 — SP Delay Element characteristics 560
Table 24-2 — Variable-length SP Delay Element Directives 561
Table 24-3 — Payload State Machine states for the MScan Scan Format 565
Table 24-4 — Ready State Machine states 566
Table 24-5 — Delay State Machine state 568
Table 25-1 — OScan SP Payload Element contents 574
Table 25-2 — Labels in Figure 25-15/TAPC state cross-reference 582

Table 25-3 — Cross reference of labels in Figure 25-16 and Figure 25-17/TAPC state 584
Table 25-4 — Payload State Machine states for the OScan Scan Format 586
Table 26-1 — HDR[2] interpretation 601
Table 26-2 — HDR[1:0] interpretation 602
Table 26-3 — SScan Scan Formats optimization summary 604
Table 26-4 — SScan0 header information and SP payload contents 605
Table 26-5 — SScan2 header information and SP payload contents 605
Table 26-6 — SScan1 header information and SP payload contents 606
Table 26-7 — SScan3 header information and SP payload contents 606
Table 26-8 — SScan1 no stalls and input-only Data Segments 608
Table 26-9 — SScan3 no stalls and input-only Data Segments 609
Table 26-10 — SScan1 no stalls and input/output Data Segment 609
Table 26-11 — SScan3 no stalls and input/output Data Segment 610
Table 26-12 — SScan2/SScan3 output-only Data Segments/no RDY bit in the SP payload 614
Table 26-13 — SScan2/SScan3 output-only Data Segments/RDY bit(s) in the SP payload 615
Table 26-14 — Cross-reference of the TAPC state labels in Figure 26-19 618
Table 26-15 — TAPC advance with Data Segments other than SScan2–SScan3 output only 622
Table 26-16 — TAPC advance with SScan2–SScan3 output-only Data Segments 622
Table 26-17 — Payload State Machine state definition 628
Table 26-18 — Escape Detection State Machine state definition 629
Table 27-1 — T5 TAP.7 function/register/command relationships 638
Table 27-2 — T5 TAP.7 register descriptions 641
Table 27-3 — PDCx_DCCy_CR0 – PDCx_DCCy_CR7 write descriptions 642
Table 27-4 — PDCx_DCCy_CR0 – PDCx_DCCy_CR7 read descriptions 643
Table 27-5 — Reset values of TAP.7 Controller registers managed with Transport Directives 644
Table 27-6 — Specifying the use of T5 TAP.7 optional functions 645
Table 27-7 — T5 TAP.7 Controller Transport Register configurations 645
Table 27-8 — DCC register configurations 645
Table 27-9 — Real TAPC state and transport relationships 648
Table 27-10 — Transport Directive nomenclature 652
Table 27-11 — Transport Directive encoding 653
Table 27-12 — Selection Directive operation (conditional relationships) 657
Table 27-13 — Register Transfer Directive operation (conditional relationships) 658
Table 27-14 — Data Transfer Directive operation (conditional relationships) 659
Table 27-15 — DCC/Data Element relationships 664
Table 28-1 — Register Element content creation 678
Table 28-2 — Register Element content utilization 679
Table 28-3 — Data Element content 682
Table 28-4 — TSM state names and encoding 685
Table 28-5 — TSM state behavior 686
Table 28-6 — PDCx/DCC interface signal functions 692
Table 28-7 — PDCx/DCC interface signal description, PDC sourced signals 693
Table 28-8 — PDCx/DCC interface signal description, DCC-sourced signals 694
Table 28-9 — PDCx/DCC interface signaling relationships 697
Table 28-10 — TP_CRR or TP_CRW Directive (eight-bit Register Element) 713
Table 28-11 — TP_DCx Directive – variable-length transfer (eight-bit Data Element) 714
Table 28-12 — TP_DCx Directive – fixed-length transfer (eight-bit Data Element) 715
Table 29-1 — Contrasting large-system applications against small-system applications 730
Table 30-1 — Scope of BSDL.7 733
Table 30-2 — BSDL.7 reserved words 735
Table 31-1 — Scope of HSDL.7 753
Table 31-2 — HSDL.7 reserved words 754
Table C-1 — TMSC drive and delay relationships 806
Table C-2 — MScan scan sequence/DR Scan (010) and IR Scan (111), delay as specified 807
Table C-3 — SP/CP combination following an MScan SP 807
Table C-4 — OScan0 scan sequence/DR Scan (010) and IR Scan (111), delay as specified 808

Table C-5 — SP/CP combination following an OScan0 SP 808
Table C-6 — OScan1 scan sequence/DR Scan (010) and IR Scan (111), delay as specified 809
Table C-7 — SP/CP combination following an OScan1 SP 809
Table C-8 — OScan2 scan sequence/DR Scan (010) and IR Scan (111) with no delay 810
Table C-9 — OScan2 scan sequence/DR Scan (010) and IR Scan (111) with delay 811
Table C-10 — SP/CP combination following an OScan2 SP 811
Table C-11 — OScan3 scan sequence/DR Scan (010) and IR Scan (111) with no delay 812
Table C-12 — OScan3 scan sequence/DR Scan (010) and IR Scan (111) with delay 813
Table C-13 — SP/CP combination following an OScan3 SP 813
Table C-14 — OScan4 scan sequence/DR Scan (010) and IR Scan (111) 814
Table C-15 — SP/CP combination following an OScan4 SP 814
Table C-16 — OScan5 scan sequence/DR Scan (010) and IR Scan (111) 815
Table C-17 — SP/CP combination following an OScan5 SP 815
Table C-18 — OScan6 scan sequence/DR Scan (010) and IR Scan (111) with no delay 816
Table C-19 — OScan6 scan sequence/DR Scan (010) and IR Scan (111) with delay 817
Table C-20 — SP/CP combination following an OScan6 SP 817
Table C-21 — OScan7 scan sequence/DR Scan (010) and IR Scan (111) with no delay 818
Table C-22 — OScan7 scan sequence/DR Scan (010) and IR Scan (111) with delay 819
Table C-23 — SP/CP combination following an OScan7 SP 819
Table C-24 — SScan0 – SP sequence following a CP/all stall profile (IN, I/O) 821
Table C-25 — SP/CP combination following an SScan0 Segment with an all SP stall profile 821
Table C-26 — SScan0 – SP sequence following a CP/all stall profile (IN, OUT) 822
Table C-27 — SScan0 – SP sequence following a CP/all stall profile (I/O, OUT) 823
Table C-28 — SScan0 – SP sequence following a CP/first stall profile (IN, I/O) 824
Table C-29 — SP/CP combination following an SScan0 segment with first SP stall profile 824
Table C-30 — SScan0 – SP sequence following a CP/first stall profile (IN, OUT) 825
Table C-31 — SScan0 – SP sequence following a CP/first stall profile (I/O, OUT) 826
Table C-32 — SScan1 – SP sequence following a CP/no stall profile (IN, I/O) 827
Table C-33 — SP/CP combination following an SScan1 segment with a no stall profile 827
Table C-34 — SScan1 – SP sequence following a CP/no stall profile (IN, OUT) 828
Table C-35 — SScan1 – SP sequence following a CP/no stall profile (I/O, OUT) 829
Table C-36 — SScan1 – SP sequence following a CP/first stall profile (I/O, OUT) 830
Table C-37 — SScan1 – SP sequence following a CP/first stall profile (IN, I/O) 831
Table C-38 — SP/CP combination following an SScan1 segment with first SP stall profile 831
Table C-39 — SScan1 – SP sequence following a CP/first stall profile (IN, OUT) transactions 832
Table C-40 — SScan1 – SP sequence following a CP/first stall profile/I/O, OUT transactions 833
Table C-41 — SScan2 – SP sequence following a CP/all stall profile (IN, I/O) 834
Table C-42 — SP/CP combination following an SScan2 segment with an all SP stall profile 834
Table C-43 — SScan2 – SP sequence following a CP/all stall profile (IN, OUT) 835
Table C-44 — SScan2 – SP sequence following a CP/all stall profile (I/O, OUT) 836
Table C-45 — SScan2 – SP sequence following a CP/first stall profile (IN, I/O) 837
Table C-46 — SP/CP combination following an SScan2 segment with first SP stall profile 837
Table C-47 — SScan2 – SP sequence following a CP/first stall profile (IN, OUT) 838
Table C-48 — SScan2 – SP sequence following a CP/first stall profile (I/O, OUT) 839
Table C-49 — SScan3 – SP sequence following a CP/no stall profile (IN, I/O) 840
Table C-50 — SP/CP combination following an SScan3 segment with a no stall profile 840
Table C-51 — SScan3 – SP sequence following a CP/no stall profile (IN, OUT) 841
Table C-52 — SScan3 – SP sequence following a CP/no stall profile (I/O, OUT) 842
Table C-53 — SScan3 – SP sequence following a CP/first stall profile (I/O, OUT) 843
Table C-54 — SScan3 – SP sequence following a CP/first stall profile (IN, I/O) 844
Table C-55 — SP/CP combination following an SScan3 segment with first SP stall profile 844
Table C-56 — SScan3 – SP sequence following a CP/first stall profile (IN, OUT) transactions 845
Table C-57 — SScan3 – SP sequence following a CP/first stall profile/I/O, OUT transactions 846
Table D-1 — TAP power and selection states viewed by the DTS 849
Table D-2 — Selection-Sequence initiation 850
Table D-3 — Selection-Sequence criteria 851

Table D-4 — Criteria for placement Online 851
Table D-5 — TAP power and selection states viewed by the DTS 852
Table D-6 — Placement of Offline-at-Start-up Online with TAPC state sequence 856
Table D-7 — TAPC state mnemonics 858
Table D-8 — Other short-form synchronization state sequences 859
Table D-9 — Configuration Register reads for TAPs [n:0] 864
Table F-1 — Factors affecting system performance and reliability 878
Table F-2 — Recommendations summary 957
Table F-3 — Recommended connection/termination schemes 960

IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture

1. Overview

1.1 Scope

The standard will define a link between IEEE 1149.1 interfaces in Debug and Test Systems (DTS) and IEEE 1149.1 (JTAG) interfaces in Target Systems (TS). The link defined by this standard introduces an additional layer between these legacy interfaces. This layer may be viewed as an adapter that provides new functionality and features while preserving all elements of the original IEEE 1149.1 (JTAG) interfaces. The standard will define the link behavior (including timing characteristics of signals), protocols, and functionality of the adapters deployed within the DTS and TS. The standard will not modify or create inconsistencies with IEEE 1149.1 (JTAG). The standard will define a superset of the IEEE 1149.1 specification and achieve compliance with IEEE Std 1149.1™-2001.[1]

1.2 Purpose

The purpose of the standard is to define a debug and test interface that meets an expanding set of challenges facing Debug and Test Systems (many of which have emerged since the inception of the original IEEE Std 1149.1) while preserving the hardware and software investments of the many industries currently using IEEE Std 1149.1-2001.

[1] Information on references can be found in Clause 2.