IEEE Std 1149.1-1990
(Includes IEEE Std1149.1a-1993)

IEEE Standard Test Access Port and Boundary-Scan Architecture

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Abstract: Circuitry that may be built into an integrated circuit to assist in the test, maintenance, and support of assembled printed circuit boards is defined. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register, such that the component is able to respond to a minimum set of instructions designed to assist with testing of assembled printed circuit boards.
Keywords: boundary-scan, boundary-scan register, circuit boards, circuitry, printed circuit boards, test ports

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The Institute of Electrical and Electronics Engineers, Inc.

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Foreword

(This foreword is not a part of IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture.)

This standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The facilities defined by the standard seek to provide a solution to the problem of testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques. They also provide a means of accessing and controlling design-for-test features built into the digital integrated circuits themselves. Such features might, for example, include internal scan paths and self-test functions as well as other features intended to support service applications in the assembled product.

Development of IEEE Standard Test Access Port and Boundary-Scan Architecture

The process of developing this standard began in 1985 when the Joint European Test Action Group (JETAG) was formed in Europe. During 1986, this group expanded to include members from both Europe and North America and, as a result, was renamed the Joint Test Action Group (JTAG). Between 1986 and 1988, the JTAG Technical Subcommittee developed and published a series of proposals for a standardized form of boundary-scan. In 1988, the last of these proposals—JTAG Version 2.0—was offered to the IEEE Testability Bus Standards Committee (P1149) for inclusion in the standard then under development. The Testability Bus Standards Committee accepted this approach. It decided that the JTAG proposal should become the basis of a standard within the Testability Bus family, with the result that the Pl149.1 project was initiated. Following these decisions, the JTAG Technical Subcommittee became the core of the IEEE Working Group that developed this standard.

Between 1985 and approval on February 15, 1990, many individuals made valuable contributions to the development of this standard. At the time of approval of this standard, the members of the working group were:

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These people were supported by many other individuals from many different organizations who contributed time, administrative effort, and technical suggestions.

In particular, the working group wishes to acknowledge the contributions made by the following individuals:

LaNae Avra	Matthias Kaufmann	David L. Rutledge
Paul Bardell	William McAnney	Wim Sauerwald
Frans P. M. Beenker	Bruno Mueller	Erwin Trischler
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Foreword to IEEE Std 1149.1a

(This foreword is not a part of IEEE Std 1149.1-1990 , IEEE Standard Test Access Port and Boundary-Scan Architecture.)

This supplement to IEEE Std 1149.1-1990 contains corrections, clarifications, and enhancements.

Corrections

Corrections are provided for errors located as a result of interaction between the developers and users of IEEE Std 1149.1-1990.

Clarifications

Interaction between developers and users of IEEE Std 1149.1-1990 highlighted parts of the original text (mostly, the descriptive material) that were ambiguous or insufficiently clear. This supplement provides clarifications that, it is hoped, will assist future users in implementing the standard.

Enhancements

Two enhancements have been made to the features defined by IEEE Std 1149.1-1990.

First, two new optional instructions have been defined—*CLAMP* and *HIGHZ*. These specifications standardize instructions that were often implemented as design-specific features on early commercial integrated circuits that claimed conformance to IEEE Std 1149.1-1990 . The provision of standard instruction names and corresponding specifications will assist in the development of design and test tools that can automatically exploit the existence of the relevant functionality.

Second, an option has been provided to switch a component from a mode in which it complies to IEEE Std 1149.1 into one in which it supports another design-for-test approach (e.g., level-sensitive scan-design for stand-alone component testing).

To assist readers already familiar with IEEE Std 1149.1-1990, paragraphs that contain changes are marked by margin bars in this supplement.

Development of This Supplement

The effort to develop this supplement was begun by the IEEE 1149.1 Working Group immediately following approval and publication of IEEE Std 1149.1-1990.

Between May 1990 and approval of this supplement on June 17, 1993, many individuals made valuable contributions. Particular thanks are due to:

Colin M. Maunder *(chair (1990) and vice-chair (1991))*
Rodham E. Tulloss *(vice-chair (1990) and chair (1991, 1992))*
Dirk van de Lagemaat *(vice-chair (Europe, 1992, 1993))*

Several individuals joined the working group as development work progressed, reflecting the growing use of IEEE Std 1149.1-1990 by industry. At the time of approval of IEEE Std 1149.1a-1993, the members of the working group were:

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Harry Bleeker
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Michel Parot
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The following persons were on the balloting committee:

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CLAUSE PAGE

IEEE Standard Test Access Port and Boundary-Scan Architecture

1. Introduction

This standard defines test logic that can be included in an integrated circuit to provide standardized approaches to:

- testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate;
- testing the integrated circuit itself; and
- observing or modifying circuit activity during the component's normal operation.

The test logic consists of a boundary-scan register and other building blocks and is accessed through a Test Access Port (TAP).

1.1 Background Reading

Persons who are not familiar with scan test and self-test techniques for digital electronic circuits may find it helpful to consult the following publications prior to reading this standard:

— AGRAWAL, V.D. and SETH, S.C., *Test generation for VLSI chips*, IEEE Computer Society Press, 1988.
— BENNETTS, R.G., *Design of testable logic circuits*, Addison-Wesley, 1984.
— EICHELBERGER, E.B. and WILLIAMS, T.W., A logic design structure for LSI testability, *Journal of Design Automation and Fault-Tolerant Computing*, vol. 2, no. 2, May 1978, pp. 165–178.
— KONEMANN, B. et al., Built-in logic block observation techniques, *Proceedings of the IEEE Test Conference*, IEEE Computer Society Press, 1979, pp. 37–41.
— MICZO, A., *Digital logic testing and simulation*, Harper & Row, 1986.

1.2 An Overview of the Operation of IEEE Std 1149.1

This clause provides a general overview of the operation of a component compatible with this standard and provides a background to the detailed discussion in later chapters.

The circuitry defined by this standard allows test instructions and associated test data to be fed into a component and, subsequently, allows the results of execution of such instructions to be read out. All information (instructions, test data, and test results) is communicated in a serial format.