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IEEE Standard for Test Access Port and Boundary-Scan Architecture

IEEE Computer Society

Sponsored by the
Test Technology Standards Committee

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IEEE Std 1149.1™-2013
(Revision of
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Abstract: Circuitry that may be built into an integrated circuit to assist in the test, maintenance and support of assembled printed circuit boards and the test of internal circuits is defined. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register, such that the component is able to respond to a minimum set of instructions designed to assist with testing of assembled printed circuit boards. Also, a language is defined that allows rigorous structural description of the component-specific aspects of such testability features, and a second language is defined that allows rigorous procedural description of how the testability features may be used.

Keywords: boundary scan, boundary-scan architecture, Boundary-Scan Description Language (BSDL), boundary-scan register, circuit boards, circuitry, IEEE 1149.1™, integrated circuit, printed circuit boards, Procedural Description Language (PDL), test, test access port (TAP), very high speed integrated circuit (VHSIC), VHSIC Hardware Description Language (VHDL)

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Introduction

This introduction is not part of IEEE Std 1149.1-2013, IEEE Standard for Test Access Port and Boundary-Scan Architecture.

This standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The facilities defined by the standard seek to provide a solution to the problem of testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques. They also provide a means of accessing and controlling design-for-test features built into the digital integrated circuits themselves. Such features might, for example, include internal scan paths and self-test functions as well as other features intended to support service applications in the assembled product.

In addition, two languages are provided to describe both the structure of the test logic and the procedures needed to use the test logic.

History of the development of this standard

The process of developing this standard began in 1985 when the Joint European Test Action Group (JETAG) was formed in Europe. During 1986, this group expanded to include members from both Europe and North America and, as a result, was renamed the Joint Test Action Group (JTAG). Between 1986 and 1988, the JTAG Technical Subcommittee developed and published a series of proposals for a standardized form of boundary scan. In 1988, the last of these proposals, JTAG Version 2.0, was offered to the IEEE Testability Bus Standards Committee (P1149) for inclusion in the standard then under development. The Testability Bus Standards Committee accepted this approach. It decided that the JTAG proposal should become the basis of a standard within the Testability Bus family, with the result that the P1149.1 project was initiated. Following these decisions, the JTAG Technical Subcommittee became the core of the IEEE Working Group that developed this standard.

After the initial approval of this standard in February 1990 and its subsequent publication, the Working Group immediately began efforts to develop a supplement for the purpose of correction, clarification, and enhancement. This effort, spurred and guided by interaction between developers and users of the original standard, culminated in IEEE Std 1149.1a™-1993, which was approved in June 1993.

The major changes to this standard introduced by IEEE Std 1149.1a-1993 were as follows:

- The addition of two optional instructions, *CLAMP* and *HIGHZ*, which standardized the names and specifications of features often implemented as design-specific features.
- The addition of an optional facility to switch a component from a mode in which it complies to this standard into one in which it supports another design-for-test approach.

Furthermore, starting with a proposal made by Kenneth P. Parker and Stig Oresjo in 1990, an effort was undertaken to develop a language to describe components that conform to this standard. This effort concluded in the approval of IEEE Std 1149.1b™-1994 in September 1994.

The major change introduced to this standard by IEEE Std 1149.1b-1994 was the addition of Annex B, which defines the Boundary-Scan Description Language. All other changes were minor and were strictly for clarification.

The 2001 revision was primarily a housekeeping update, designed to incorporate learning from the first 10 years of the standard’s use into the standard document. The principal changes introduced were as follows:

- To reduce the risk of accidental entry into test mode, the requirement that a binary code for the *EXTEST* instruction be {000...0} was removed and use of this binary code for other instructions that result in entry to test mode was deprecated.

- To increase the flexibility with which instructions may be implemented and merged, the implicitly merged *SAMPLE/PRELOAD* instruction was redefined as two separate instructions: *SAMPLE* and *PRELOAD*. *These instructions can continue to share a single binary code*, effectively resulting in a merged *SAMPLE/PRELOAD* instruction, but alternatively, they may now share binary codes with other instructions, provided that no rules applying to any of the merged instructions are violated.
- To enable more efficient implementation of boundary-scan register cells provided at system logic outputs, the source of data to be captured in such cells in response to the *SAMPLE* instruction was allowed to be at the connected system pin. Additionally, three new cell types based on this implementation (**BC_8, BC_9,** and **BC_10**) were added to the standard Boundary-Scan Description Language (BSDL) Package and Package Body.
- To permit more flexible boundary-scan register cell implementations, sharing of circuitry between the boundary-scan register and other elements of the test and/or system logic were allowed in limited cases.
- To support more complete description of IC pin drivers with bus keeper circuits, a new value for <disable result> was defined (**KEEPER**).
- To track the widespread acceptance of BSDL, the language was made a normative part of this standard and its use for documentation was mandated.

Additionally, a number of minor changes were made to correct and clarify the language of this standard.

Changes introduced by this revision

First, this version of the standard affirms what had been required in the previous (2001) version. There are only minor clarifications or relaxations to the rules that are already established. It is expected that components currently compliant with the previous version of this standard will remain compliant with this one. The one exception is that the previously deprecated **BC_6** boundary-scan cell is no longer supported or defined, and the component supplier must provide a user-supplied BSDL package defining the **BC_6** cell for any component using the **STD_1149_1_2013** standard Package and still using that cell.

Second, while this is a major revision, items introduced in this version are optional and intended to provide test improvements for the complex components being created today and in the foreseeable future. There are also significant improvements in documentation capability, including the introduction of a new language to document test procedures unique to the component.

The major changes, listed in the order in which they appear in this standard, are as follows:

In the standard body:

- A new, optional, test mode persistence controller that can maintain the IEEE 1149.1 test logic in test mode even if the active instruction does not force test mode. Clause 6 is now split into 6.1 for the TAP controller and 6.2 for the test mode persistence controller. In support of this new controller, there are three new instructions: *CLAMP_HOLD* and *TMP_STATUS* in 8.20, with the new TMP status test data register in Clause 16; and *CLAMP_RELEASE* in 8.20.
- A new, optional *ECIDCODE* instruction in 8.15 and its electronic chip identification test data register in Clause 13 to supplement the existing *IDCODE* and *USERCODE* instructions and allow for the recovery of an Electronic Chip Identification value used to identify and track individual integrated circuits.
- A new, optional, component initialization mechanism to provide more flexibility in preparing the component for test. The *INIT_SETUP, INIT_SETUP_CLAMP,* and *INIT_RUN* instructions in 8.17, 8.18, and 8.19, and their new initialization data and initialization status test data registers in Clause 14 and Clause 15, respectively. This will allow programmable input/output (I/O) to be set up prior to board or system testing, as well as any tasks required to put the system logic into a safe state for test.
- A new, optional, *IC_RESET* instruction in 8.21 and its reset_select test data register in Clause 17 to provide control of component reset functions through the TAP.

- In 9.2, an optional standard TAP to test data register interface is recommended, and examples of different types of test data register cells using this interface are shown. In addition, the concept of register segments is expanded to allow for segments that may be excluded or included. This is introduced to support power domains that may be powered down, and yet may have a segment of a test data register within that domain. However, the capability was kept general.
- In the new 9.4, the rules for defining and controlling the new excludable and selectable segments are established.
- Boundary-scan register description in Clause 11 has been updated to support:
  i) Optional excludable (but not selectable) boundary-scan register segments
  ii) Optional observe-only boundary-scan register cells to redundantly capture the signal value on all digital pins except the TAP pins
  iii) Optional observe-only boundary-scan register cells to capture a fault condition on all pins, including nondigital pins, except the TAP pins
- Documentation requirements in Clause 18 have been updated for the new capabilities.

Note that where rules were removed or moved in this version of this standard, a placeholder was left behind ("Removed in this version ...." or "Moved to Permision ....") in order to preserve the rule numbering from previous versions. This is intended to simplify the transition for both users and tool vendors in supporting what is a significant change.

In Annex B (Boundary Scan Description Language):

- The entire annex was rewritten for:
  i) Increased clarity of what was normative versus descriptive text
  ii) Increased consistency in presentation
- BSDL is no longer a "proper subset" of VHDL, but it is now "based on" VHDL. See B.4. In particular, new pin type keywords were introduced in B.8.3 that are not needed in VHDL but give a more accurate description of each port in BSDL.
- Formal definitions of language elements are included in B.5 instead of reliance on inheritance from VHDL.
- Some changes to the BNF notation used, including definition of all the special character tokens, are in B.6.
- Pin mapping in B.8.7 now allows for documenting that a port is not connected to any device package pin in a specific mapped device package.
- The boundary-scan register description in B.8.14 introduces new attributes for defining boundary-scan register segments, and introduces a requirement for documenting the behavior of an undriven input.
- New capabilities are introduced for documenting the structural details of test data registers:
  i) Subclause B.8.18 introduces the definition of mnemonics that may be associated with register fields.
  ii) Subclause B.8.19 introduces the ability to name fields within a register or segment.
  iii) Subclause B.8.20 introduces the ability to define the types of cells used in a test data register (TDR) field.
  iv) Subclause B.8.21 introduces the ability to hierarchically assemble segments into larger segments or whole registers.
  v) Subclause B.8.22 introduces the ability to define constraints on the values to be loaded in a register or register field.
  vi) Subclause B.8.23 introduces the ability to associate a register field or bit to specific ports and other information, and to associate a power port to other ports.
- The role of a User Defined Package defined in B.10 has been expanded to support logic IP providers who may need to document test data register segments contained within their IP.

A new annex, Annex C, codifies the Procedural Description Language (PDL), a new language for documenting the procedural and data requirements for some of the new instructions. As mentioned, this version of the standard introduces new instructions for configuring complex I/Os prior to entering the *EXTEST* instruction. As the data required for initialization could vary for each use of the component on each distinct board or system design, this created the need for a new language for setting internal TDR register fields in order to configure the I/O. It was decided to adopt PDL and tailor it to the BSDL register descriptions and IEEE 1149.1 needs.

A new informative annex, Annex D, shows extended examples of BSDL and PDL used together to describe the structure and the procedures for use of new capabilities.

A new informative annex, Annex E, shows example pseudo-code for the execution of the PDL iApply command, the most complex of the new commands in PDL.

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1. Overview

1.1 Scope

This standard defines test logic that can be included in an integrated circuit to provide standardized approaches to:

- Testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate
- Testing the integrated circuit itself
- Observing or modifying circuit activity during the component's normal operation

The test logic consists of a boundary-scan register and other building blocks and is accessed through a test access port (TAP).

1.2 Purpose

1.2.1 Overview of the operation of this standard

This subclause provides a general overview of the operation of a component compatible with this standard and provides a background to the detailed discussion in later clauses.

The circuitry defined by this standard allows test instructions (which take control of the component outputs and observe the component inputs) and associated test data to be fed into a component and, subsequently, allows the results of execution of such instructions to be read out. All information (instructions, test data, and test results) is communicated in a serial format.

The sequence of operations would be controlled by a bus master, which could be either an automatic test equipment (ATE) or a component that interfaces to a higher level test bus as a part of a complete system maintenance architecture. Control is achieved through signals applied to the test mode select (TMS) and test clock (TCK) inputs of the various components connected to the bus master. Starting from an initial state in which the test circuitry defined by this standard is inactive, a typical sequence of operations would be as follows.