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IEEE Standard for Memory Modeling in Core Test Language (CTL)

IEEE Computer Society

Sponsored by the
Test Technology Standards Committee

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IEEE Std 1450.6.2™-2014

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of the
IEEE Computer Society

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Abstract: Reuse of test data and test structures developed for individual cores (designs) when integrated into larger integrated circuits is required for system-on-chip (SoC) tests. This standard defines language constructs sufficient to represent the context of a memory core and of the integration of that memory core into an SoC. This facilitates the development and reuse of test and repair mechanisms for memories. This standard also defines constructs that represent the test structures internal to the memory core for reuse in the creation of the tests for the logic outside the memory core. Semantic rules are defined for the language to facilitate interoperability between different entities (the memory core provider, the system integrator, and the automation tool developer) involved in the creation of an SoC. The capabilities are an extension of IEEE Std 1450.6™-2005. As a result of this extension, CTL's limitations of handling memories are addressed.

Keywords: core test language (CTL), IEEE 1450.6.2™, memory built-in self-test (memory BIST), memory modeling, memory repair, standard test interface language (STIL), system-on-chip (SoC)

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Introduction

This introduction is not part of IEEE Std 1450.6.2™-2014, IEEE Standard for Memory Modeling in Core Test Language (CTL).

The core test language (CTL) defined in IEEE Std 1450.6™-2005 is a modeling language created to enable design reuse for system-on-chip flows (or SoC flows). The base CTL standard does not address all memory-specific characteristics and structural information required to create memory test and repair patterns. This extension of CTL adds support for modeling memories.

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IEEE Standard for Memory Modeling in Core Test Language (CTL)

1. Overview

1.1 General

Memory core test language (memory CTL) is an extension of the core test language (CTL, or IEEE Std 1450.6™-2005) that allows the description of the test-related aspects of memory blocks. CTL is a language created for a system-on-chip flow (or SoC flow), where a design created by one group is reused as a sub-design of a design created by another group. Memory CTL extends this capability to the special requirements of memory blocks embedded in a larger design of logic circuitry. For further information on CTL, consult IEEE Std 1450.6™-2005.[1]

Test of memory blocks embedded into an SoC requires access to these memory blocks, or to logic circuitry capable of testing the memory blocks. Memory CTL does not describe the tests, access through the SoC, or the testing circuitry. Rather, it describes the memory blocks themselves so that the SoC designer can provide the test and test mechanisms. After this provision, the main CTL standard may be used to describe the memory blocks in the context of the SoC. memory CTL is intended as extension of CTL for the purpose of facilitating the development of high coverage memory tests.

This standard defines language constructs sufficient to represent the test and repair-relevant aspects of memory blocks, including their capabilities to facilitate testing outside of the blocks.

[1] Information on references can be found in Clause 2.