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IEEE Standard for High-Speed Test Access Port and On-Chip Distribution Architecture

IEEE Computer Society

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Test Technology Standards Committee

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IEEE Std 1149.10™-2017

IEEE Standard for High-Speed Test Access Port and On-Chip Distribution Architecture

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of the
IEEE Computer Society

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Abstract: Circuitry that may be built into an integrated circuit to assist in the test, maintenance, and support of assembled printed circuit boards, assembled multi-die packages, and the test of die internal circuits is defined in this standard. The circuitry includes a high-speed TAP (HSTAP) with a packet encoder/decoder and distribution architecture through which instructions and test data are communicated. The standard leverages the languages of IEEE Std 1149.1™ to describe and operate the on-chip circuits.

Keywords: 3D-IC, Boundary-Scan Description Language, BSDL, debug, High Speed JTAG, I2C, IEEE 1149.1™, PDL, IEEE 1149.10™, integrated circuit, JTAG, wafer, Procedural Description Language, SERDES, SPI, system level test

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Introduction

This introduction is not part of IEEE Std 1149.10™-2017, IEEE Standard for High-Speed Test Access Port and On-Chip Distribution Architecture.

With the approval of IEEE Std 1149.1™-2013, the industry now has a standardized approach to hierarchical design-for-test. IEEE Std 1149.1-2013 provides access to IP blocks via IEEE 1500 wrapper serial ports. IEEE 1149.1 package files and PDL standardized how to describe IP block operation destined for SoC integration. Some Working Group members started to discuss the bandwidth limitations of the IEEE 1149.1 TAP, the limitations of single scan-in/scan-out for test time, the diminishing single-ended I/O count for parallel scan due to die-stacking, and the desire for leveraging PDL to be re-used beyond the TAP. A group of interested parties was formed in August of 2013. C. J. Clark presented the fundamentals on the HSTAP, PEDDA, and Packet format at the first meeting. Industry-based SERDES packets were discarded because they required storing packet information in memory and generally required more on-chip resources. The IEEE 1149.10 architecture needed to be simple and easy to add on to the mission mode design. A PAR was approved in October 2013. A publicly available history of the Working Group's attendance, motions, minutes, and presentations can be found at http://grouper.ieee.org/groups/1149/10/.

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1. Overview

1.1 Scope

This standard defines a high speed test access port for delivery of test data, a packet format for describing the test payload, and a distribution architecture for converting the test data to/from on-chip test structures.

The standard re-uses existing high speed I/O (HSIO) known in the industry for the high speed test access port (HSTAP). The HSIO connects to an on-chip distribution architecture through a common interface. The scope includes the distribution architecture test logic and packet decoder logic. The objective of the distribution architecture and packet decoder is that it can be readily re-used with different integrated circuits (ICs) that host different HSIO technology, such that the standard addresses as large a part of the industry as possible.

The scope includes IEEE 1149.1 Boundary-Scan Description Language (BSDL) and Procedural Description Language (PDL) documentation, which can be used for configuring a mission mode HSIO to a test mode compatible with the HSTAP. The same BSDL and PDL can then be used to deliver high-speed data to the on-chip test structures.

1.2 Need

Test time has always been an important metric for system on a chip (SoC). The original IEEE 1149.1 test access port is fine for simple board interconnect tests, but as on-chip operations via the IEEE 1149.1 test access port (TAP) have increased, the use of the IEEE 1149.1 TAP becomes inefficient for board test and on-board field programmable gate array (FPGA) configuration. Large FPGAs take tens of minutes to configure through the IEEE 1149.1 TAP. The IEEE 1149.1 TAP has always been too slow for production SoC test. Wide test access mechanisms (TAMs) are used to increase test throughput during production IC test at the cost of requiring more tester resources. Wide TAMs are also not useful for test re-use at the board/system level because many of the I/O of the TAM are not accessible. Pin limitations also exist where the pins required for the IEEE 1149.1 TAP cannot be supported by a small package or die. A high-speed test access port and packet encoder/decoder and distribution architecture (PEDDA) is needed by the industry to standardize a faster test data delivery mechanism for IC automatic test equipment (ATE), but also be re-usable at board and system level test. Today, in 2017, to get 10 Gbit/s data transfer on a die