BS EN 62433-2:2017

BSI Standards Publication

EMC IC modelling

Part 2: Models of integrated circuits for EMI behavioural simulation - Conducted emissions modelling (ICEM-CE) (IEC 62433-2:2017)

bsi.

National foreword

This British Standard is the UK implementation of EN 62433-2:2017. It is identical to IEC 62433-2:2017. It supersedes BS EN 62433-2:2010, which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

A list of organizations represented on this committee can be obtained on request to its secretary.

This publication does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

© The British Standards Institution 2017
Published by BSI Standards Limited 2017

ISBN 978 0 580 89669 9

ICS 31.200; 33.100.10

Compliance with a British Standard cannot confer immunity from legal obligations.

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 30 November 2017.

Amendments/corrigenda issued since publication

Date	Text affected

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 62433-2

May 2017

ICS 31.200; 33.100.10

Supersedes EN 62433-2:2010

English Version

EMC IC modelling - Part 2: Models of integrated circuits for EMI behavioural simulation - Conducted emissions modelling (ICEM-CE) (IEC 62433-2:2017)

Modèles de circuits intégrés pour la CEM - Partie 2: Modèles de circuits intégrés pour la simulation du comportement lors de perturbations électromagnétiques - Modélisation des émissions conduites (ICEM-CE) (IEC 62433-2:2017)

EMV-IC-Modellierung - Teil 2: Modelle integrierter Schaltungen für die Simulation des Verhaltens bei elektromagnetischer Beeinflussung - Modellierung leitungsgeführter Aussendungen (ICEM-CE) (IEC 62433-2:2017)

This European Standard was approved by CENELEC on 2017-03-03. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Serbia, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Avenue Marnix 17, B-1000 Brussels

© 2017 CENELEC All rights of exploitation in any form and by any means reserved worldwide for CENELEC Members.

European foreword

The text of document 47A/999/FDIS, future edition 2 of IEC 62433-2, prepared by SC 47A "Integrated circuits", of IEC/TC 47 "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62433-2:2017.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2017-12-03
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2020-03-03

This document supersedes EN 62433-2:2010.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 62433-2:2017 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 61967	NOTE	Harmonized in EN 61967 series.
IEC 61967-4	NOTE	Harmonized as EN 61967-4.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

Publication	Year	Title	EN/HD	Year
IEC/TS 62433-1	2011	EMC IC modelling - Part 1: General modelling framework	-	-
CISPR 17	-	Methods of measurement of the suppression characteristics of passive EMC filtering devices	EN 55017	-

This page deliberately left blank

CONTENTS

FOREWORD 7
1 Scope 9
2 Normative references 9
3 Terms, definitions, abbreviations and conventions 9
3.1 Terms and definitions 9
3.2 Abbreviations 11
3.3 Conventions 11
4 Philosophy 11
4.1 General 11
4.2 Conducted emission from core activity (digital culprit) 12
4.3 Conducted emission from I/O activity 12
4.4 Data exchange format 12
5 ICEM-CE basic components 13
5.1 General 13
5.2 Internal Activity (IA) 13
5.2.1 General 13
5.2.2 Examples of IA 14
5.3 Passive Distribution Network (PDN) 14
5.3.1 General 14
5.3.2 Examples of PDN 15
6 IC macro-models 16
6.1 Types of IC macro-models 16
6.2 General IC macro-model 16
6.3 Block-based IC macro-model 17
6.3.1 Block component 17
6.3.2 Inter-Block Coupling component (IBC) 18
6.3.3 Block-based IC macro-model structure 19
6.4 Sub-model-based IC macro-model 21
6.4.1 Sub-model component 21
6.4.2 Sub-model-based IC macro-model structure 22
7 CEML format 23
7.1 General 23
7.2 CEML structure 24
7.3 Global keywords 24
7.4 Header section 24
7.5 Lead definitions 25
7.6 SPICE macro-models 26
7.7 Validity section 28
7.7.1 General 28
7.7.2 Attribute definitions 29
7.8 PDN 31
7.8.1 General 31
7.8.2 Attribute definitions 32
7.8.3 Description 36
7.9 IBC 40
7.9.1 General 40

7.9.2 Attribute definitions 40
7.10 IA 42
7.10.1 General 42
7.10.2 Attribute definitions 42
7.10.3 Description 46
8 Requirements for parameter extraction 47
8.1 General 47
8.2 Environmental extraction constraints 47
8.3 IA parameter extraction 47
8.4 PDN parameter extraction 47
8.5 IBC parameter extraction 48
Annex A (normative) Preliminary definitions for XML representation 49
A.1 XML basics 49
A.1.1 XML declaration 49
A.1.2 Basic elements 49
A.1.3 Root element 49
A.1.4 Comments 50
A.1.5 Line terminations 50
A.1.6 Element hierarchy 50
A.1.7 Element attributes 50
A.2 Keyword requirements 50
A.2.1 General 50
A.2.2 Keyword characters 51
A.2.3 Keyword syntax 51
A.2.4 File structure 51
A.2.5 Values 53
Annex B (normative) CEML valid keywords and usage 56
B.1 Root element keywords 56
B.2 File header keywords 57
B.3 Validity section keywords 58
B.4 Global keywords 59
B.5 Lead Keyword 59
B.6 Lead_definitions section attributes 60
B.7 Macromodels section attributes 60
B.8 Pdn section keywords 61
B.8.1 Lead element keywords 61
B.8.2 Netlist section keywords 63
B.9 Ibc section keywords 63
B.9.1 Lead element keywords 63
B.9.2 Netlist section keywords 65
B.10 Ia section keywords 65
B.10.1 Lead element keywords 65
B.10.2 Voltage section keywords 66
B.10.3 Current section keywords 68
Annex C (informative) Example of ICEM-CE macro-model in CEML format 70
C.1 General 70
C.2 PDN and IBC sub-model 70
C.3 IA sub-model 71

C.4 Frequency domain ICEM-CE in CEML 73
C.5 Time domain ICEM-CE in CEML 75
Annex D (informative) Conversions between parameter types 77
D.1 General 77
D.2 Conversion for one-port PDN 77
D.3 Conversion for two-port PDN 77
Annex E (informative) Model parameter generation 79
E.1 General 79
E.2 Default structure and values 79
E.2.1 General 79
E.2.2 IA parameters 79
E.2.3 PDN parameters 80
E.3 Model parameter generation from design information 81
E.3.1 General 81
E.3.2 IA parameters 81
E.3.3 PDN parameters 85
E.4 Model parameter generation from measurements 87
E.4.1 IA parameters 87
E.4.2 PDN parameters 90
Annex F (informative) Decoupling capacitors optimization 100
Annex G (informative) Conducted emission prediction 102
Annex H (informative) Conducted emission prediction at PCB level 103
Bibliography 105

Figure 1 – Decomposition example of a digital IC for conducted emissions analysis 12
Figure 2 – IA component in the case of a current source 13
Figure 3 – Example of IA characteristics in the time domain 14
Figure 4 – Example of IA characteristics in the frequency domain 14
Figure 5 – Example of a four-terminal PDN using lumped elements 15
Figure 6 – Example of a seven-terminal PDN using distributed elements 16
Figure 7 – Example of a twelve-terminal PDN using matrix representation 16
Figure 8 – General IC macro-model 17
Figure 9 – Example of block component with a single IA 18
Figure 10 – Example of block components for I/Os 18
Figure 11 – Example of IBC with four internal terminals 19
Figure 12 – Relationship between blocks and IBC 19
Figure 13 – Block-based IC macro-model 20
Figure 14 – Example of block-based IC macro-model 21
Figure 15 – Example of simple sub-model 21
Figure 16 – Sub-model-based IC macro-model 22
Figure 17 – CEML inheritance hierarchy 23
Figure 18 – Example of a netlist file defining a sub-circuit 28
Figure 19 – PDN represented as S-parameters in Touchstone format 38
Figure 20 – Simulated IA waveform with corresponding parameters 45
Figure A.1 – Multiple XML (CEML) files 52

Figure A.2 – XML files with data files (*.dat) 52
Figure A.3 – XML files with additional files 53
Figure C.1 – Example pin-out of a microcontroller and the modelled pins 70
Figure C.2 – PDN sub-model topology 71
Figure C.3 – IA sub-model topology 72
Figure C.4 – IA of digital block in frequency domain 72
Figure C.5 – IA of digital block in time domain 73
Figure E.1 – Typical characterization current gate schematic 82
Figure E.2 – Current peak during switching transition 82
Figure E.3 – Example of IA extraction procedure from design 83
Figure E.4 – Technology Influence 83
Figure E.5 – Final current waveform for a program period 84
Figure E.6 – Comparison between measurement and simulation 84
Figure E.7 – Example lumped element model of a package 85
Figure E.8 – Circuit structure of the netlist 87
Figure E.9 – Principle of the IA computation in the frequency domain 88
Figure E.10 – Process involved to model $i_A(t)$ 89
Figure E.11 – $i_{Ext}(t)$ measured using IEC 61967-4 89
Figure E.12 – $i_A(t)$and $i_{Ext}(t)$ profiles 90
Figure E.13 – Conventional one-port S-parameter measurement 90
Figure E.14 – Two-port method for low impedance measurement 91
Figure E.15 – Two-port method for high impedance measurement 91
Figure E.16 – Example of a hardware set-up used to extract the PDN parameters 92
Figure E.17 – Miniature 50 Ω coaxial connectors 93
Figure E.18 – Impedance probe using two miniature coaxial connectors 93
Figure E.19 – Open and short terminations 93
Figure E.20 – Measurement probe model 94
Figure E.21 – De-embedding principle 94
Figure E.22 – Example of a predefined PDN structure 95
Figure E.23 – RL configuration 96
Figure E.24 – RLC configuration 97
Figure E.25 – RLC with magnetic coupling configuration 97
Figure E.26 – Impedance seen from Vcc and Gnd 97
Figure E.27 – Complete PDN component 98
Figure E.28 – Set-up for correlation (left), measurement and prediction model (right) 99
Figure E.29 – Set-up used to measure the internal decoupling capacitor 99
Figure F.1 – Equivalent schematic of the complete electronic system 100
Figure F.2 – Impedance prediction and measurements 101
Figure G.1 – IEC 61967-4 test set-up standard 102
Figure G.2 – Comparison between prediction and measurement 102
Figure H.1 – Prediction of ETVddc noise level at PCB level 103
Figure H.2 – Good agreements on the noise envelope 104

Table 1 – Attributes of Lead keyword in the *Lead_definitions* section 25
Table 2 – Compatibility between the Mode and Type fields for correct CEML annotation 26
Table 3 – *Subckt* definition 26
Table 4 – Definition of the *Validity* section 28
Table 5 – Definition of the Lead keyword for *Pdn* section 32
Table 6 – Valid data formats and their default units in the *Pdn* section 35
Table 7 – Valid file extensions in the Pdn section 35
Table 8 – Valid fields of the Lead keyword in the *Pdn* section 36
Table 9 – *Netlist* definition 39
Table 10 – Differences between the *Pdn* and *Ibc* section fields 41
Table 11 – Valid fields of the *Lead* keyword for IBC definition 41
Table 12 – Definition of the *Lead* keyword in the *Ia* section 42
Table 13 – *Voltage* and *Current* definition 43
Table 14 – Valid file extensions in the *Ia* section 43
Table 15 – Definition of the *Pulse* keyword in the *Voltage* or *Current* section 44
Table 16 – Base units of the Pulse section's fields 44
Table 17 – Valid data formats and their default units for the *Voltage* and *Current* elements 46
Table A.1 – Valid logarithmic units 54
Table D.1 – One-port conversion 77
Table D.2 – Two-port conversion 78
Table E.1 – Typical parameters for CMOS logic technologies 80
Table E.2 – Typical number of logic gates vs. CPU technology 80
Table E.3 – R, L and C parameters for various package types 81
Table E.4 – Measurement configurations and extracted RLC parameters 95

INTERNATIONAL ELECTROTECHNICAL COMMISSION

_____

EMC IC MODELLING –

Part 2: Models of integrated circuits for EMI behavioural simulation – Conducted emissions modelling (ICEM-CE)

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62433-2 has been prepared by subcommittee 47A: Integrated Circuits, of IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition published in 2008. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

Incorporation of an XML based exchange format for model representation.

The text of this standard is based on the following documents:

FDIS	Report on voting
47A/999/FDIS	47A/1007/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62433 series, published under the general title *EMC IC modelling*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

EMC IC MODELLING –

Part 2: Models of integrated circuits for EMI behavioural simulation – Conducted emissions modelling (ICEM-CE)

1 Scope

This part of IEC 62433 specifies macro-models for an Integrated Circuit (IC) to simulate conducted electromagnetic emissions on a printed circuit board. The model is commonly called Integrated Circuit Emission Model – Conducted Emission (ICEM-CE).

The ICEM-CE macro-model can also be used for modelling an IC-die, a functional block and an Intellectual Property (IP) block.

The ICEM-CE macro-model can be used to model both digital and analogue ICs.

Basically, conducted emissions have two origins:

- conducted emissions through power supply terminals and ground reference structures;
- conducted emissions through input/output (I/O) terminals.

The ICEM-CE macro-model addresses those two types of origins in a single approach.

This standard defines structures and components of the macro-model for EMI simulation taking into account the IC's internal activities.

This part of IEC 62433 has two main parts:

- the first is the electrical description of ICEM-CE macro-model elements along with the specific requirements for information.
- the second part proposes a universal data exchange format called CEML based on XML. This format allows encoding the ICEM-CE in a more useable and generic form for simulating the conducted emissions.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC TS 62433-1:2011, *EMC IC modelling – Part 1: General modelling framework*

CISPR 17, *Methods of measurement of the suppression characteristics of passive EMC filtering devices*

3 Terms, definitions, abbreviations and conventions

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.