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IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks

IEEE Computer Society

Sponsored by the
Test Technology Standards Committee

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USA

IEEE Std 1149.6™-2015
(Revision of
IEEE Std 1149.6-2003)

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Abstract: IEEE Std 1149.1™ is augmented by this standard to improve the ability for testing differential and/or ac-coupled interconnections between integrated circuits on circuit boards and systems.

Keywords: ac-coupled signaling, boundary scan, circuit boards, differential signaling, IEEE 1149.6™, integrated circuits, interconnect test, printed circuit boards, test

This standard is dedicated to the memory of our friend and colleague, Carl Barnhart. This was Carl's standard from start to finish. Carl was our leader and mentor. We will dearly miss his passion, humor and vast knowledge.

The Institute of Electrical and Electronics Engineers, Inc.
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Introduction

This introduction is not part of IEEE Std 1149.6-2015, IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks.

History of the development of this standard

The development of this standard was started on 21 May 2001 by an ad hoc industry Working Group called by Agilent Technologies[1] and Cisco Systems. This group formulated this standard with the intention of handing it over to the IEEE for formal standardization when the underlying technology became understood.

The group adopted as its mission: To define, document, and promote a means for designing integrated circuits (ICs) that support robust boundary-scan testing of boards where signal pathways make use of differential signaling and/or ac-coupled technologies. This technology utilizes and is compatible with the existing IEEE Std 1149.1[2]. The goal is to upgrade the capabilities of IEEE Std 1149.1 to maintain the rapid and accurate detection and diagnosis of interconnection defects in boards and systems despite the fault-masking effects of differential signaling and the dc blocking effects of ac-coupled signaling.

The group first referred to itself as the "AC EXTEST" Working Group, but has since expanded its charter to consider topics now called "Advanced I/O."

Changes introduced by this revision

A summary of the changes includes the following:

- Deletion of Annex E content
- Changes driven by the 2013 update to IEEE Std 1149.1
- Added new level-detection behavior to the test receiver for ac-coupled channels
- Documentation of driver and test receiver analog parameters, including documenting programmability of those parameters
- Programmability of coupling capacitor shunts
- Documentation of non-compliance of certain pins to EXTEST_PULSE performance
- Addition of Procedure Description Language (PDL) routines for documenting the procedures to access programmable analog parameters
- IP Package support in Boundary-Scan Description Language (BSDL)
- New "AC" boundary register cell designs

This revision affirms what has been required from the previous version, and products that conform to the previous version are still compliant with this revision. There is one deletion: Annex E (informative) proposed an "Initialize" instruction. This topic has since been subsumed into IEEE Std 1149.1-2013.

Many of the changes found in this revision are in response to the major revision of the underlying IEEE 1149.1 standard that was released in 2013. This standard introduced new concepts, such as segmented data registers, the initialization data register, and register descriptions. These concepts, once adopted in new ICs,

[1] Now called Keysight Technologies.
[2] Information on references can be found in Clause 2.

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will materially affect the design, and subsequent description in BSDL, for those devices that are to conform to this standard.

There are also changes that come from industry commentary and usage practices developed over the past decade. A known problem exists in the 2003 version of this standard for level-sensitive behavior when using the EXTEST instruction defined in IEEE Std 1149.1. Simply, in some cases it is impossible to ensure compatible drive and receive voltage levels. When a channel is guaranteed to be ac-coupled, and the only use for the EXTEST instruction is to detect a shorted capacitor, there is a new behavior defined that essentially performs a simple but robust continuity check. See option 2) of rule a) in 6.2.2.1.

A significant addition provided by this revision is the ability to provide for (and describe) variable, programmable parameters such as threshold and common mode voltages. This will assist the users of test generation and diagnosis tools in creating and debugging tests, where analog parameter mismatches could occur.

On-chip ac coupling capacitors can now have provisions to shunt them out of the input signal pathway under control of the test circuitry. Improvements are offered to the ability to test external (board level) capacitors for shorts and to compensate for mismatches in voltages between devices.

It is recognized in this revision that for some pins, it may not be possible for the EXTEST_PULSE instruction to transmit or receive data due to dynamic conditioning of the associated circuitry that is not fully completed by a single data pulse; that is, a longer set of transitions, such as that provided by EXTEST_TRAIN, may be required. Such pins that need this exception can now be identified in BSDL so that tools can make appropriate tradeoffs for them.

The 2013 revision of IEEE Std. 1149.1 also added a new PDL, which is used to describe how devices and their registers are used for various testing purposes. This revision requires the documentation of certain programmable features, when implemented in a device, in PDL.

The 2013 revision of IEEE Std. 1149.1 made significant additions to BSDL, which affect the BSDL representation of 1149.6 technology as described in Clause 7. Part of these changes are driven by the electronics industry’s movement towards the usage of intellectual property packages, where portions of circuitry are bought and sold for inclusion in other IC designs. This means that, along with the circuitry description, any relevant test-oriented information about IEEE 1149.1 or IEEE 1149.6 implementations contained within such IP must also be provided in BSDL packages. Thus, significant changes for such support are found in Clause 7 — see 7.4 and 7.5, taking note of “Port Behavior” descriptions. New and updated examples for both BSDL and PDL appear in Clause 7.

Annex C contains information on ac boundary register cell designs. Two new cells [AC_40 and AC_41 (see C.9)] are documented there.

Updating BSDL to the new standard

Components compliant with the 2003 version of this standard will typically be compliant with this new version. However, the BSDL documentation must be updated. First, the BSDL will need to be updated to comply with the changes introduced in IEEE Std 1149.1-2013, including as a minimum:

- Changing all “Linkage” pin types to the new linkage and power pin types in the port declaration.
- Updating “Use” and component conformance statements to STD_1149_1_2013.
- Adding an <input spec> for all pins of type "input" in the Boundary-Scan Register description.
- Taking advantage of the optimal register structural descriptions (REGISTER_MNEMONICS, REGISTER_FIELDS, REGISTER_ASSEMBLY, etc.) and of the PDL language to document

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programmable characteristics of the component that could not be documented in a standard form before. This would be particularly valuable when documenting any initialization built into the component and required for proper operation of the I/O and boundary tests.

Second, the BSDL will need to be updated to comply with the changes introduced by this standard:

— Updating AIO component conformance statement to STD_1149_6_2015.

— Adding to the AIO_Pin_Behavior attribute the new parameters for driver common-mode and peak-to-peak voltages, test receiver threshold and hysteresis voltages, bypass control of on-chip capacitors, and any ports that require the EXTEST_TRAIN instruction.

— Adding PDL procedures to document initialization of any programmable I/O parameters. This ties into the new initialization documentation introduced in IEEE Std 1149.1-2013.

A component compliant with IEEE Std 1149.1-2001 and IEEE Std 1149.6-2003 may have included proprietary capabilities for initializing I/O, including advanced I/O. If the capabilities are conformant to the new requirements of these standards, then they must be documented in order to be compliant. However, even if those proprietary capabilities are not conformant, if they can be made public by writing procedures in PDL using the reserved PDL procedure names where appropriate, doing so will improve the automation of test generation and execution.

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IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks

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1. Overview

1.1 Scope

This standard defines extensions to IEEE Std 1149.1™ to standardize the boundary-scan structures and methods required to help ensure simple, robust, and minimally intrusive boundary-scan testing of advanced digital networks.[1] Such networks are not adequately addressed by existing standards, especially for those networks that are ac-coupled, differential, or both. Testing enabled by this standard will operate in parallel with IEEE Std 1149.1 testing of conventional digital networks and in conjunction with IEEE Std 1149.4™ testing of conventional analog networks. This standard also specifies software and Boundary-Scan Description Language (BSDL) extensions to IEEE Std 1149.1, which are required to support new I/O test structures.

1.2 Purpose

Existing boundary-scan test standards (IEEE Std 1149.1, IEEE Std 1149.4) do not fully address some of the increasingly common, newer digital network topologies, such as ac-coupled, differential interconnections on very high speed (1+ Gb/s) digital data paths. IEEE Std 1149.1 structures and methods are intended to test static (dc-coupled), single-ended networks. They are unable to test dynamic (ac-coupled) digital networks, since ac coupling blocks static signals. Differential networks are also inadequately tested by

[1] Information of references can be found in Clause 2.

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